	I3C		I3C Basic		
Feature	v1.0	v1.1.1/v1.2	v1.0	v1.1.1 /v1.2	**Mandatory / Optional**
Dynamic Address Assignment	✓	✓	✓	✓	Mandatory[1]
Common Command Codes (CCCs)	✓	✓	✓	✓	Mandatory
Specified 1.2V-3.3V Operation for 50pf C load	✓	✓	✓	✓	Mandatory[1]
Target Reset	-	✓	-	✓	Mandatory
Error Detection and Recovery	✓	✓	✓	✓	Mandatory
Controller Role Request	✓	✓	✓	✓	Mandatory[2]
12.5 MHz SDR (Controller, Target and Legacy I2C Target Compatibility)	✓	✓	✓	✓	Optional[3]
In-Band Interrupt (w/MDB)	✓	✓	✓	✓	Mandatory[2]
Hot-Join Mechanism	✓	✓	✓	✓	Mandatory[2]
Secondary Controller	✓	✓	✓	✓	Mandatory
Specified 1.0V Operation for 100pf C load	-	-/✓	✓	✓	Optional
Set Static Address as Dynamic Address CCC (SETAASA)	-	✓	✓	✓	Optional
Synchronous Timing Control	✓	✓	-	-	Optional
Asynchronous Timing Control (Mode 0)	✓	✓	-	✓	Optional
Asynchronous Timing Control (Mode 1-3)	✓	✓	-	-	Optional
HDR-DDR	✓	✓	-	✓	Optional
HDR-TSL/TSP	✓	✓	-	-	Optional
HDR-BT (Multi-Lane Bulk Transport)	-	✓	-	✓	Optional
Grouped Addressing	-	✓	-	✓	Optional
Device-to-Device(s) Tunneling	-	✓	-	-	Optional
Multi-Lane for Speed (Dual/Quad for SDR and HDR-DDR)	-	✓	-	-	Optional
Monitoring Device Early Termination	-	✓	-	-	Optional
Availability	MIPI members only		Public		

Notes: [1] At least one option must be supported. [2] Mandatory for Controller and Optional for Target. [3] Optional but recommended.