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Intel
Addressing 5G RF- FE Control Challenges with MIPI RFFE^SM^ v3.0
Agenda

• Problem Statement
  – Abstract 5G sub 6 GHz RF Front End
  – Use case with tight Tx timing
  – Use case with tight Rx timing

• Solutions
  – Strategies to solve the trigger congestion problem
  – How to separate the trigger programming from the actual triggering
  – Revised use cases using timed triggers

• Timed Trigger Design Topics
  – Designing an RFFE master controller
  – Designing an RFFE slave controller

• Mappable Triggers (an additional feature)

• Questions
5G RF-FE Control

• Timing & Requirements
Abstract 5G Sub 6 GHz, RF Front End (RFFE)

Frequency Range 1 RFFE

- **Receive**
  - 4x4 DL MIMO
  - Inter-band Down Link Carrier Aggregation (DL CA)

- **Transmit**
  - 2x2 UL MIMO and/or
  - Inter-band Up Link Carrier Aggregation (UL CA)
  - PAs with Envelope Tracking (EnvTr)

RFFE Control Architecture

- Number of buses to be limited
  - ideally: 1
  - in reality: several

**Command Sequences (CS) to various Front End components interfere!**
Use Case with Tight Tx Timing: 2*UL Carrier Aggregation

UL #1 Symbol N-1

Cyclic Prefix

UL #1 Symbol N

PA/EnvTr #1 prog. CS

PA #1 Trig

EnvTr # 1 Trig

1.2µs @ SCS 60kHz

UL #2 Symbol N-1

CP

UL #2 Symbol N

EnvTr/PA #2 prog. CS

EnvTr #2 Trig

PA #2 Trig

0.65µs 34 clock cycles

Congestion! Triggers displaced / Symbols corrupted

RFFE traffic #1

UL #1 @ ANT_1

RFFE traffic #2

UL #2 @ ANT_2

Common RFFE bus Command Sequence
Use Case with Tight Rx Timing: X*DL Carrier Aggregation

Symbol corruption occurs if Duration ‘D’ ≤ X * 0.65µs

≤ 33 µs (MRTD by 3GPP)

DL @ ANT

Common RFFE Command Sequence

LNA\textsubscript{1} prog
LNA\textsubscript{2} prog
LNA\textsubscript{X} prog
LNA\textsubscript{X} Trig
LNA\textsubscript{1} Trig
LNA\textsubscript{2} Trig

34 SCLK

0.65µs
Potential Solution (Hardware)

• How to solve the RFFE bus congestion
• Duplicating resources
Duplicated RFFE Buses

Spatial Solution

- Concurrently operated FE components shall not share a common bus
- Requires to know ALL use cases in advance
- Worst case: 1 bus per component
- Very costly in PCB area and routing

Not flexible for future requirements
Potential Solution (Programmable)

• How to solve the RFFE bus congestion with Timed Trigger(s)
Timed Trigger – Solution in Time (1)

- Trigger delay up to 510 clock cycles (~10µs @ 52MHz)

Max Clock
52MHz

D = T₂ – T₁
Timed Trigger – Solution in Time (2)

Calculate the time ‘D’ from the end of Timed Trigger CS to the time the trigger should fire.

(a) Timed Trig CS ($D_1$)

(b) Timed Trig CS ($D_2$)

(c) Timed Trig CS ($D_3$)

$D_1 = T_1 - T_a$

$D_2 = T_2 - T_b$

$D_3 = T_3 - T_c$
Design Topics

• How to design RFFE bus clients and masters
Adding Timed Triggers to RFFE Master Controller

List of timed RFFE actions
- Timed Action @ T1
- Timed Action @ T2
- Timed Action @ T3

RFFE Scheduler

TT#1 CS
T1-Ta

TT#2 CS
T2-Tb

TT#3 CS
T3-Tc

RFFE Dispatcher + SCLK Maintainer

keep clock alive

SCLK

SDAT
Adding Timed Triggers to RFFE Client Controller

**Timed Triggers**
- Is an add-on to Extended Triggers as in v2.1
- Counter: Count down from ‘D’ with each SCLK cycle; if ≠0
- Transition from 1 to 0; fire trigger (Timer expired)
Mappable Triggers

• Problem to be solved
• Design issues
Problem: fixed assignment Trigger $\rightarrow$ UDR Register (Set)

EXT_TRIG_MASK

EXT_TRIG

$\text{EXT\_TRIG\_MASK} \rightarrow_1 \text{UDR Shadow Register X} \rightarrow_1 \text{UDR Register X}$

$\text{EXT\_TRIG} \rightarrow_1 \text{UDR Shadow Register Y} \rightarrow_1 \text{UDR Register Y}$

Fixed (HW) assignments
UDR Register (Set) per LUT assigned to Trigger

EXT_TRIG_MASK

EXT_TRIG

M10 M9 M8 M7 M6 M5 M4 M3

≥1

LUT

≥1

Mapping X (UDR)

UDR Register X

Mapping Y (UDR)

UDR Register Y

Configurable assignments

UDR Shadow Register X

UDR Shadow Register Y
Summary With Key Takeaway Messages

• Timed Triggers can reduced the number of RFFE busses

• Mappable Triggers can allow flexible mapping of Front End hardware to reduce the number of RFFE connection