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Hardent

Next-Generation Mobile, AR/VR, & Automotive Displays With VESA VDC-M & MIPI® DSI-2™

Mipi Alliance Developers Conference
Taipei
18 October 2019
Bandwidth Challenge for Video Connectivity
Gap between transport bandwidth and display requirements is increasing.
Possible Solutions vs. Trade-offs

1. Add transport lanes
   - More pins/cables needed
   - Real estate increase
   - Weight increase
   - Cost increase
   - Power consumption increase
   - EMI noise increase

2. Use video compression
   - Potential visual artifacts
   - Greater design complexity
   - Increased latency
Industry Compression Timeline

Proprietary Compression Technologies

DSC 1.1

DSC 1.2a

2012 2014 2016 2018
Display Stream Compression (DSC) Overview

- Visually lossless video compression standard
- Up to **3x** compression (8 bpp) without any perceptible differences
- Extremely low latency (< 0.5 usec)
- Video quality excellent with all types of content
  - Natural and test images, text, and graphics
- Requires a single line of pixel storage + rate buffer
  - Intra-frame Variable Bit Rate Encoder
  - Constant Bit Rate (CBR) transmission
  - Based on Delta Pulse Code Modulation (DPCM)
  - Mid Point (MPP), Block Predictor (BP)
  - Modified Median Adaptive Predictor (MMAP)
  - Indexed Color History (ICH)

Source diagram: VESA DSC white paper
Transport Standards Using DSC

- MIPI DSI® 1.3.1
- DisplayPort 1.4
- DisplayPort 2.0
- USB Type-C
- HDBT 2.0
- HDMI 2.1
- eDP 1.4b
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Applications Using DSC

- Mobiles
- Tablets
- GPUs
- AR/VR head-mounted displays
- In-car video systems
- Video transport
- UHD / 8K TVs
- DTV STBs
- High-resolution monitors

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Some Applications Require **Even More Bandwidth**

**Mobile Displays**
- Need to support gaming
- Need to be “AR/VR ready”
- Require higher display resolutions & frame rates

**AR/VR Displays**
- Need to drive two displays
- Require higher pixel density (ppi) & frame rates

**Automotive Displays**
- Are increasing rapidly
- Require higher display resolutions
Product Display Bandwidth Trends

VDC-M = VESA Display Compression for Mobile
# DSC vs. VDC-M

<table>
<thead>
<tr>
<th></th>
<th>DSC</th>
<th>VDC-M</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Encoding Block Structure</strong></td>
<td>3x1 pixels</td>
<td>8x2 pixels</td>
</tr>
<tr>
<td><strong>Encoding Tools</strong></td>
<td>Mid Point (MPP)</td>
<td>Mid Point (MPP)</td>
</tr>
<tr>
<td></td>
<td>Block Predictor (BP)</td>
<td>Enhanced Block Predictor (BP)</td>
</tr>
<tr>
<td></td>
<td>Modified Median Adaptive Predictor (MMAP)</td>
<td>Transform (DCT and Hadamard)</td>
</tr>
<tr>
<td></td>
<td>Indexed Color History (ICH)</td>
<td>Enhanced Quantization</td>
</tr>
<tr>
<td><strong>Visually Lossless Performance</strong></td>
<td>8 bpp (bits per pixel)</td>
<td>5-6 bpp (bits per pixel)</td>
</tr>
<tr>
<td><strong>IC Complexity</strong></td>
<td>Low</td>
<td>Medium</td>
</tr>
<tr>
<td><strong>RAM Usage</strong></td>
<td>Single line</td>
<td>2.5 lines</td>
</tr>
<tr>
<td><strong>Latency (end-to-end)</strong></td>
<td>&lt;0.5us</td>
<td>&lt;1.2us</td>
</tr>
<tr>
<td><strong>(UHD 3840x2160 example)</strong></td>
<td>&lt;2H line</td>
<td>&lt;5H line</td>
</tr>
<tr>
<td><strong>Pixels / Clock Architecture</strong></td>
<td>Encoder 1</td>
<td>Decoder 2</td>
</tr>
<tr>
<td></td>
<td>Decoder 3</td>
<td>Decoder 4</td>
</tr>
</tbody>
</table>
VDC-M Enhanced Block Prediction Mode

- Block prediction is performed on 2x1 or 2x2 partitions
  - One block prediction vector (BPV) for all color components of each partition
- Block prediction uses a large and regular search area
  - 64 potential BPVs for each partition
VDC-M New Transform Mode

• Transforms residuals of best of 8 intra-predictors
  – DC, Vertical, Vertical Left, Vertical Right, Diagonal Left, Diagonal Right, Horizontal Left, Horizontal Right

• Transform is done for each color component on 8x2 block (or 4x2 block for YUV 4:2:x chroma)
  – Uses Butterfly DCT in horizontal direction and Hadamard transform in vertical direction
  – Separates higher frequencies (which the eye is less sensitive to) from lower frequencies
  – Similar transform to what is done in MPEG and JPEG encoding
Transport Standards Using VDC-M

• VDC-M was officially released in May 2018

• MIPI Alliance adopted VDC-M 1.2 as part as their new DSI-2 v1.1 specification

• VDC-M is now being considered by other transport specifications
Mobile Market Trends

- Mobile devices need to be VR-ready
- Movement from LCD to OLED displays
  - Ultra-high resolutions and pixel density (up to 1500 ppi)
  - High dynamic range
  - Higher frame rate
  - Optical compensation
  - Foldable, rollable displays
  - Lower power consumption
  - Non-uniformity compensation
- DDIC frame buffer going from 10 to 100 Mbits

<table>
<thead>
<tr>
<th></th>
<th>2010</th>
<th>2020</th>
</tr>
</thead>
<tbody>
<tr>
<td>Display Resolution</td>
<td>1280 x 720</td>
<td>3840 x 2160</td>
</tr>
<tr>
<td>Frame Rate</td>
<td>60 fps</td>
<td>120 fps</td>
</tr>
<tr>
<td>Pixel Depth</td>
<td>24 bits</td>
<td>30 bits</td>
</tr>
<tr>
<td>Interface</td>
<td>0.5 Gbps / lane</td>
<td>2.0 Gbps / lane</td>
</tr>
<tr>
<td>Display Bandwidth</td>
<td>1.3 Gbps</td>
<td>29.9 Gbps</td>
</tr>
</tbody>
</table>
Use Case: Mobile and Tablet Applications

- Application processor
- DDIC (Display Driver IC) and touch panel controller
- Benefits
  - Reduce bandwidth
  - Save power
  - Save on cost
  - Lower EMI
VDC-M Mobile/Tablet Use Case

- Additional DSI lane saving
- Power consumption saving
- Smaller SDRAM frame buffer

Examples

- WQUXGA Display (2400x3840) 24bpp 60fps
  - D-PHY<sup>SM</sup> 2.5Gbps: only 2 lanes required
  - SDRAM 4 times smaller

- UHD Display (2160x3840) 30bpp 120fps
  - D-PHY 2.5Gbps: only 3 lanes required
  - SDRAM 5 times smaller

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AR/VR Market

- **Console market**
  - Oculus, HTC Vive, Sony Playstation, Windows MR,...
  - Cables are running out of bandwidth
    - Requires 2 displays at higher resolution, higher ppi, higher refresh rates

- **Standalone market**
  - Microsoft Hololens, Google Daydream, Oculus Go, HTC Vive Focus,...
  - Bandwidth, power management, and miniaturization are huge obstacles
  - Optimized silicon is emerging
    - Qualcomm Snapdragon XR, ARM Mali-D77, NVidia Tegra

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Use Case: AR/VR Head-Mounted Display

Applications
- Video capture
- Application processor and GPU
- Micro-display driver IC

Benefits
- Lower bandwidth
- Smaller RAM buffer
- Power and $ savings
- Low latency

Untethered AR System With Frame Buffer

Game Console - Wired VR System
VDC-M to Fulfill Future AR/VR Requirements

VESA members AR/VR Task Group Survey Summary

1. Resolutions per eye will increase over time from 2K x 2K in 2019 to **8K x 8K in 2025**

2. It is believed that very few people see a difference beyond 8K x 8K per eye
   a. This is about **60 pixels per degree** for 273 degrees horizontally
   b. It allows 220 degrees plus 25 degrees of overlap between the eyes

3. Refresh rates required is between **120 to 240Hz** to meet human perception limits

4. Pixel resolution of 12bpc will be required by 2025

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**AR/VR Use Cases & VDC-M**

- All resolutions/frame rates below are “per eye”

<table>
<thead>
<tr>
<th>Transport</th>
<th>Transport Bandwidth Available</th>
<th>DSC 8bpp</th>
<th>VDC-M 6bpp</th>
<th>VDC-M 5bpp</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 Gbits/sec</td>
<td>19.3 Gbits/sec</td>
<td>2.8Kx2.8K 120Hz</td>
<td>4Kx4K 100Hz</td>
<td>4Kx4K 120Hz</td>
</tr>
<tr>
<td>2 lanes</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10 Gbits/sec</td>
<td>38.7 Gbits/sec</td>
<td></td>
<td>4Kx4K 120Hz</td>
<td>5Kx5K 120Hz</td>
</tr>
<tr>
<td>4 lanes</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>20 Gbits/sec</td>
<td>38.7 Gbits/sec</td>
<td>4Kx4K 120Hz</td>
<td>5Kx5K 120Hz</td>
<td>5Kx5K 120Hz</td>
</tr>
<tr>
<td>2 lanes</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>20 Gbits/sec</td>
<td>77.3 Gbits/sec</td>
<td>5Kx5K 120Hz</td>
<td>8Kx8K 100Hz</td>
<td>8Kx8K 120Hz</td>
</tr>
<tr>
<td>4 lanes</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Digital Car Market

- Number of displays in cars is increasing rapidly
  - ADAS, infotainment, control panels, rear seat displays, head-up displays, side and rear view mirrors, ...
  - 1-3 displays → 10-12 displays
  - 1 camera → 5-10 cameras
  - 2-5 sensors → 10-20 sensors

<table>
<thead>
<tr>
<th>Display Type</th>
<th>Spatial Resolution</th>
<th>DPI (pix / inch)</th>
<th>Bandwidth Req. @ 60 Hz refresh</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mid-range car</td>
<td>HD 1280 x 720</td>
<td>100</td>
<td>1.8 Gbps</td>
</tr>
<tr>
<td>High-end car</td>
<td>FHD 1920 x 1080</td>
<td>200</td>
<td>3.6 Gbps</td>
</tr>
<tr>
<td>Next-gen. car</td>
<td>UHD 3860 x 2160</td>
<td>400</td>
<td>14.4 Gbps</td>
</tr>
</tbody>
</table>
Automotive Transport Link Technologies Today

- Several technologies available: Maxim GMSL, Inova APIX, Valens HDBaseT, TI FPD-Link

- Link speed ranges between 1.0 - 6.0 Gbps typically over a 15 meter coaxial or shielded twisted pair cable

- Automotive environment is demanding: higher bitrate (> 6 Gbps) adds significant challenges
  - Electromagnetic noise immunity, reliability, cost, etc.
  - Adoption/certification of high-speed serial link technology is a long & expensive process
  - Using multiple links per screen is expensive
More Cables Is NOT The Solution

- Wiring harness is the 3rd highest cost component in a car (behind engine and chassis) comprising 50% of the cost of labor for the entire car
- 3rd heaviest component (after the chassis and engine)*
- EMI and signal integrity is a major challenge

* Source: Delphi, Inc.
In-Car Video Applications

- Benefits
  - Smaller bandwidth for multiple feeds
  - Low latency
  - Save on expensive cabling
  - Lower EMI
Compressed Multi-Stream Transport

- **Cable #1**
  - Stream A - Frame 1
  - Stream A - Frame 2
  - Stream A - Frame 3

- **Cable #2**
  - Stream B - Frame 1
  - Stream B - Frame 2
  - Stream B - Frame 3

- **Cable #3**
  - Stream C - Frame 1
  - Stream C - Frame 2
  - Stream C - Frame 3

**Video Compression**

- **Single Cable**
  - Stream A - Frame 1
  - Stream A - Frame 2
  - Stream A - Frame 3
  - Stream B - Frame 1
  - Stream C - Frame 1
  - Stream A - Frame 2
  - Stream C - Frame 2
  - Stream B - Frame 2
  - Stream A - Frame 3
  - Stream B - Frame 3
  - Stream C - Frame 3

- **Packet Based**
  - Stream A - Frame 1
  - Stream A - Frame 2
  - Stream A - Frame 3
  - Stream B - Frame 1
  - Stream B - Frame 2
  - Stream B - Frame 3
  - Stream C - Frame 1
  - Stream C - Frame 2
  - Stream C - Frame 3

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VDC-M Automotive Use Case

• Number of displays in cars is increasing rapidly

• Display physical size may not increase due to car physical limitation, but resolution is increasing
  – High-end displays now support FHD (150-200 ppi)
  – Next-generation aiming at UHD (300-400 ppi)

• VDC-M extends life cycle of existing link technology
  – Limitations to increase transmission link speed between head unit and multiple displays
  – Automotive environment is demanding, higher bitrate (> 6Gbps) adds significant challenges
    • Electromagnetic noise immunity, reliability, cost, etc.
  – Adoption/certification of high-speed serial link technology is a long and expensive process
  – Using multiple links per screen is expensive
  – Potential use of self-healing ring cuts available link bandwidth
Use Cases: Display / Link Compression Requirements

- Projected automotive link speed in the future = 12 Gbps
- Future display requirements:
  - 12 UHD displays
  - Bandwidth per display = 600 MPixels/sec = 14.4 Gbps for 24-bit pixels

<table>
<thead>
<tr>
<th>Compression</th>
<th>Target bpp</th>
<th>Comp. Factor</th>
<th>Bandwidth Req.</th>
<th># of UHD Displays / Links</th>
<th># of Links Required For 12 Displays</th>
</tr>
</thead>
<tbody>
<tr>
<td>Uncompressed</td>
<td>24</td>
<td>1X</td>
<td>14.4 Gbps*</td>
<td>1 or 2</td>
<td>12 or 24</td>
</tr>
<tr>
<td>VESA DSC</td>
<td>8</td>
<td>3X</td>
<td>4.8 Gbps</td>
<td>2</td>
<td>6</td>
</tr>
<tr>
<td>VESA VDC-M</td>
<td>6</td>
<td>4X</td>
<td>3.6 Gbps</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>4.8X</td>
<td>3.0 Gbps</td>
<td>4</td>
<td>3</td>
</tr>
</tbody>
</table>

* Slightly exceeds available bandwidth
Is it safe?

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Automotive Functional Safety

- Governed by **ISO 26262** - Functional Safety for Road Vehicles standard
- 4 safety levels: ASIL A (lowest) to ASIL D (highest)

<table>
<thead>
<tr>
<th></th>
<th>ASIL B</th>
<th>ASIL C</th>
<th>ASIL D</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single Point Fault Metric</td>
<td>&gt; 90%</td>
<td>&gt; 97%</td>
<td>&gt; 99%</td>
</tr>
<tr>
<td>Latent Fault Metric</td>
<td>&gt; 60%</td>
<td>&gt; 80%</td>
<td>&gt; 90%</td>
</tr>
<tr>
<td>Probabilistic Metric for Hardware Failures</td>
<td>&lt; 10^{-7}/h</td>
<td>&lt; 10^{-7}/h</td>
<td>&lt; 10^{-8}/h</td>
</tr>
</tbody>
</table>
Example: Head Unit Display

- Display shows a video coming from a backup camera

- Safety Goals for the end-to-end video path (hardware level):
  - Safety goal #1: stream displayed has no corrupted pixels
  - Safety goal #2: stream displayed has no frozen frame
Video Encoder Safety Mechanisms

- Internal Safety Diagnostic Mechanisms
  - Fault avoidance mechanism
    - Reset performed at the beginning of every frame
  - Additional circuits added to the compression IP core (in blue)
    - Self Check
    - Control output diagnostics (Output Check)
    - RAM ECC correctable and uncorrectable errors
    - Configuration register protection (Config Check)

- External Safety Diagnostic Mechanisms
  - Offers maximum reliability
  - Implemented to protect against faults not detected by the internal safety mechanisms, e.g.:
    - Interrupt pin validation
    - Frame start/done monitoring
    - Test of internal safety mechanisms
    - Watermark video frames (detects frozen frames)
Conclusion

• There is a clear need within the industry for the additional bandwidth savings offered by VDC-M compression

• VDC-M is already supported by MIPI DSI-2℠
  – VDC-M will be supported by other transport technologies in the future

• The VDC-M compression algorithm is complex
  – Each application has its own unique requirements

• Visit our demo in the exhibitor area to see a live VDC-M demo & find out more about using compression in your next design

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ADDITIONAL RESOURCES

• VESA Website
  https://vesa.org/vesa-display-compression-codecs

• MIPI Website
  https://www.mipi.org/specifications/dsi-2

• Hardent Website
  – https://www.hardent.com/ip-products-vdc-m/
THANK YOU