Imaging interface advancements and development to meet the needs of mobile and mobile-influenced industries
Brief overview from Peter Lefkin
Managing Director, MIPI Alliance
About MIPI Alliance

We are a global, collaborative organization comprised of over 280 member companies spanning the mobile and mobile-influenced ecosystems.

MIPI Alliance is leading innovation in mobile interface technology.
Active Technical Working Groups

- Camera
- Debug
- Display
- Low Latency Interface
- Low Speed Multipoint Link
- PHY (C/D/M)
- Reduced Input Output
- RF Front End
- Sensor / I3C<sup>SM</sup>
- Software
- Test
- UniPro<sup>SM</sup>
MIPI Alliance continues to evolve its Roadmap to meet the needs of the mobile and mobile-influenced industry with new and revised specifications.
Overview

Generational advancements and development of MIPI CSI imaging interface to meet the needs of Mobile and beyond applications including:

• Two equally capable MIPI imaging interface architectures
  – CSI-2 over C/D-PHYs
  – CSI-3 over UniPro and M-PHY

• Provision to mitigate PSD emissions
• Extended Virtual Channels
• High Dynamic Range enhancements
• Latency Reduction and Transport Efficiency
• Always On Metadata and Pixel Transfer
• Differential Pulse Code Modulation
Two equally capable imaging interface architectures

- **CSI-2** protocol contains transport and application layers, and natively supports: C-PHY, D-PHY, or combo C/D-PHY

- **CSI-3** application stack connects to UniPro transport layer, which in turn bolts onto M-PHY
**CSI-2 D-PHY 1.2 extension**
- Pix BW scales linearly
  - 2.5 Gbps Channel delivers 10 Gbps over 4 data lanes and a clock lane (10 D-PHY pins).

**CSI-2 C-PHY 1.0 extension**
- Pix BW benefit from log₂5 mapping gain
  - 2.5 Gbps Channel delivers 17.1 Gbps over 3 lanes (9 C-PHY pins), or 22.7 Gbps over 4 lanes (12 C-PHY pins).

**CSI-3 application stack**
- Connects to UniPro and M-PHY
  - Supports networking features using fixed gear channel rates of up to 5.8 Gbps.
  - Rev control may run lower rate if asymmetric gears are supported by Image Sensor and Application Processor.
### 4K @ 30 fps and 12 BPP using CSI-2

<table>
<thead>
<tr>
<th>Required MIPI Specs (IPs)</th>
<th>Required PHY pins</th>
<th>Required Lane Rate</th>
<th>Required BW</th>
<th>Variable Link Rate</th>
<th>Control Interface</th>
</tr>
</thead>
<tbody>
<tr>
<td>[CSI-2] [D-PHY]</td>
<td>6</td>
<td>1.78 Gbps</td>
<td>3.56 Gbps</td>
<td>Yes</td>
<td>I2C</td>
</tr>
<tr>
<td>[CSI-2] [C-PHY]</td>
<td>3</td>
<td>1.55 Gbps</td>
<td>3.56 Gbps</td>
<td>Yes</td>
<td>I2C</td>
</tr>
</tbody>
</table>

### 4K @ 30 fps and 12 BPP using CSI-3

<table>
<thead>
<tr>
<th>Required MIPI Specs (IPs)</th>
<th>Required PHY pins</th>
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<th>Required BW</th>
<th>Variable Link Rate</th>
<th>Control Interface</th>
</tr>
</thead>
<tbody>
<tr>
<td>[CSI-3] [UniPro] [M-PHY]</td>
<td>4</td>
<td>5.0 Gbps</td>
<td>3.56 Gbps</td>
<td>No</td>
<td>In-band</td>
</tr>
</tbody>
</table>
Evolution of CSI-2 Performance Capabilities
Image Sensor @ 60 fps

- CSI-2 v1.3
- CPHY v1.0 @ 2.5 Gbz
- (22.7 Gbps over 12 wires)

- CSI-2 v1.2
- DPHY v1.2 @ 2.5 Gbz (10 Gbps over 10 wires)
- (25.3 Gbps over 11 wires)

- CSI-2 v1.1
- DPHY v1.1 @ 1.5 Gbz (6 Gbps over 10 wires)
- (17 Gbps over 9 wires)

- Achieves 34 Gbps using 18 wires; and beyond with scaling
- Optimal Pixel-Rate matched to Link Rate with C/D-PHY conduits
- Achieves 20 Gbps using 18 wires with scaling

Gen1
Gen2
CSI-2 Benefits of Embedded Clock & Data

- Multiple port configurations are required to map Imaging Use Cases
- CSI-2 v1.3 provides Logical Port realizations with embedded clock & data
CSI-2 over C-PHY (N-Phase) Data Path

**Triode Data Path**

**Transmitter**
Take in 16 bits, generate 7 symbols

- 16-bit to 7-symbol Mapper
- Parallel-to-Serial
- Symbol Encoder, 3-Phase Driver

21 = 7 symbols, 3 FRP bits each. 3 bits define one of 5 state transitions

**Channel**

- Channel with 3-phase polarity-encoded symbols for each 16-bit word
- Each symbol has five possible states
- The change on ABC from one symbol to the next defines the symbol value

**Receiver**
Receive 7 symbols, output 16 bits

- 3-Phase Receiver, Symbol Decoder
- Serial-to-Parallel
- 7-symbol to 16-bit De-Mapper
- 16-bit word output

**Transmission sequence of a 16-bit word**

- MSB: 78
- LSB: 9a

**Mapper**

- Seven FRP Commands

**“A” to “B” (x state)**

- Master side
- Slave side

- R_AB, R_BC, R_CA

**Mpi True Area**

- MPA, MPA
- MPA, MPA
- MPA, MPA
N-Phase (CSI-2 over C-PHY): 6 states using 3 wires
## N-Phase: 5 Transition arcs

<table>
<thead>
<tr>
<th>Trio State</th>
<th>Wire Amplitude</th>
<th>Receiver diff input voltage</th>
<th>Receiver digital output</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>A</td>
<td>B</td>
<td>C</td>
</tr>
<tr>
<td>+x</td>
<td>+V</td>
<td>0</td>
<td>+V/2</td>
</tr>
<tr>
<td>-x</td>
<td>0</td>
<td>+V</td>
<td>+V/2</td>
</tr>
<tr>
<td>+y</td>
<td>+V/2</td>
<td>+V</td>
<td>0</td>
</tr>
<tr>
<td>-y</td>
<td>+V/2</td>
<td>0</td>
<td>+V</td>
</tr>
<tr>
<td>+z</td>
<td>0</td>
<td>+V/2</td>
<td>+V</td>
</tr>
<tr>
<td>-z</td>
<td>+V</td>
<td>+V/2</td>
<td>0</td>
</tr>
</tbody>
</table>

### 3Ph Trio Arcs

- 
  - Y: W/2, V: 0, V: 0.5±0.5
  - Z: V/2, V: 0, V: 0.5±0.5
  - X: 0, V: V/2, V: 0.5±0.5
  - X: 0, V: V/2, V: 0.5±0.5
<table>
<thead>
<tr>
<th>Byte</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>0x0000</td>
</tr>
<tr>
<td>0x01</td>
<td>0x0000</td>
</tr>
<tr>
<td>0x02</td>
<td>0x0000</td>
</tr>
<tr>
<td>0x03</td>
<td>0x0000</td>
</tr>
<tr>
<td>0x04</td>
<td>0x0000</td>
</tr>
<tr>
<td>0x05</td>
<td>0x0000</td>
</tr>
<tr>
<td>0x06</td>
<td>0x0000</td>
</tr>
<tr>
<td>0x07</td>
<td>0x0000</td>
</tr>
<tr>
<td>0x08</td>
<td>0x0000</td>
</tr>
<tr>
<td>0x09</td>
<td>0x0000</td>
</tr>
<tr>
<td>0x0A</td>
<td>0x0000</td>
</tr>
<tr>
<td>0x0B</td>
<td>0x0000</td>
</tr>
<tr>
<td>0x0C</td>
<td>0x0000</td>
</tr>
<tr>
<td>0x0D</td>
<td>0x0000</td>
</tr>
<tr>
<td>0x0E</td>
<td>0x0000</td>
</tr>
<tr>
<td>0x0F</td>
<td>0x0000</td>
</tr>
</tbody>
</table>

Legend for abbreviated bit values above:
- r0 = Rotate[0]
- p0 = Polarity[0]
- r1 = Rotate[1]
- p1 = Polarity[1]
- r2 = Rotate[2]
- p2 = Polarity[2]
- r3 = Rotate[3]
- p3 = Polarity[3]
- r4 = Rotate[4]
- p4 = Polarity[4]
- r5 = Rotate[5]
- p5 = Polarity[5]
- r6 = Rotate[6]
- p6 = Polarity[6]
### N-Phase: Example of CSI-2 pixel data to C-PHY signaling 1/2

<table>
<thead>
<tr>
<th>16-bit Pix Data hex</th>
<th>16-bit Pix Data decimal</th>
<th>Mapping to symbols over 7 UI Region</th>
<th>Encoding to Wire State State</th>
<th>A</th>
<th>B</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>789a 30874</td>
<td>40; 4K</td>
<td>2 0 1 0</td>
<td>+x</td>
<td>V</td>
<td>0</td>
<td>V/2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2 0 1 0</td>
<td>+y</td>
<td>V/2</td>
<td>V</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 0 0 1</td>
<td>+z</td>
<td>0</td>
<td>V/2</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4 1 0 0</td>
<td>-y</td>
<td>V/2</td>
<td>0</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2 0 1 0</td>
<td>+y</td>
<td>V/2</td>
<td>V</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 0 0 0</td>
<td>+z</td>
<td>0</td>
<td>V/2</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2 0 1 0</td>
<td>+z</td>
<td>0</td>
<td>V/2</td>
<td>V</td>
</tr>
<tr>
<td>bcde 48350</td>
<td>40; 1K</td>
<td>4 1 0 0</td>
<td>-z</td>
<td>V</td>
<td>V/2</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2 0 1 0</td>
<td>-x</td>
<td>0</td>
<td>V</td>
<td>V/2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3 0 1 1</td>
<td>+y</td>
<td>V/2</td>
<td>V</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 0 0 1</td>
<td>-x</td>
<td>0</td>
<td>V</td>
<td>V/2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4 1 0 0</td>
<td>+x</td>
<td>V</td>
<td>0</td>
<td>V/2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3 0 1 1</td>
<td>-y</td>
<td>V/2</td>
<td>0</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 0 0 0</td>
<td>-x</td>
<td>0</td>
<td>V</td>
<td>V/2</td>
</tr>
</tbody>
</table>
N-Phase: Example of CSI-2 pixel data to C-PHY signaling 2/2
N-Phase Mission Critical Transfers 1/2

- **32-bit PACKET HEADER (PH)**
- **C-PHY Packet Data**
- **16-bit PACKET FOOTER (PF)**

**PH**
- Reserved
- Data ID
- 16-Bit Word Count (l.s. byte first)
- 16-Bit PH Checksum (l.s. byte first)

**C-PHY Packet Data**
- Data 0
- Data 1
- Data 2
- Data 3
- Data WC-4
- Data WC-3
- Data WC-2
- Data WC-1

**PF**
- 16-bit Checksum (l.s. byte first)

**Total Packet Byte Count**
- Lane 1: $2n$
- Lane 1: $2n+1$

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### N-Phase mission critical transfers 2/2

#### Link Error Example (a): Loss of No Symbol Clocks

<table>
<thead>
<tr>
<th>Symbol Interval</th>
<th>TX: Transmit ESCAPE[^0:6]</th>
</tr>
</thead>
<tbody>
<tr>
<td>s0  s1  s2  s3  s4  s5</td>
<td>3  4  4  4  4  3  2  4  3</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Transmitted Symbols</th>
<th>2  1  3  2  1  3  0  3  4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmitted Wire States</td>
<td>+z  -x  -z  +x  +y  -x  +y  +x  -y</td>
</tr>
<tr>
<td>Received Wire States</td>
<td>+z  -x  -z  +x  +y  -x  +y  +z  -y</td>
</tr>
<tr>
<td>Received Symbols</td>
<td>2  1  3  2  1  3  0  3  4</td>
</tr>
</tbody>
</table>

#### Link Error Example (b): Loss of One Symbol Clock

<table>
<thead>
<tr>
<th>Symbol Interval</th>
<th>TX: Transmit ESCAPE[^0:6]</th>
</tr>
</thead>
<tbody>
<tr>
<td>s0  s1  s2  s3  s4  s5</td>
<td>3  4  4  4  4  3  0  3  1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Transmitted Symbols</th>
<th>1  3  0  3  4  1  4  3  4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmitted Wire States</td>
<td>+z  +z  +y  -x  +z  -x  +z  -z  +x  -z</td>
</tr>
<tr>
<td>Received Wire States</td>
<td>+z  +z  +y  -z  +z  -z  +z  -z  -x  -x</td>
</tr>
<tr>
<td>Received Symbols</td>
<td>1  3  0  3  4  1  1  2  4</td>
</tr>
</tbody>
</table>

#### Link Error Example (c): Loss of Two Symbol Clocks

<table>
<thead>
<tr>
<th>Symbol Interval</th>
<th>TX: Transmit ESCAPE[^0:6]</th>
</tr>
</thead>
<tbody>
<tr>
<td>s0  s1  s2  s3  s4  s5</td>
<td>4  3  1  2  0  1  1  3  4  4</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Transmitted Symbols</th>
<th>4  3  1  2  0  1  1  3  4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmitted Wire States</td>
<td>+z  -z  +x  -x  -x  -z  +y  +y  -y  +z  +y  +y  +z  -z</td>
</tr>
<tr>
<td>Received Wire States</td>
<td>+z  -z  +x  -x  -x  -z  +y  +y  -y  +z  +y  +y  +z  -z</td>
</tr>
<tr>
<td>Received Symbols</td>
<td>4  3  1  2  0  1  1  2  4</td>
</tr>
</tbody>
</table>

**Notes:**
- Symbols are transmitted serially from left to right
- Wire state and symbol errors are highlighted in yellow
- ▲: point at which symbol clock is lost
- ▲: point at which symbol clock is restored
- ◆: point of incorrect word alignment
- ◆: point at which correct word alignment is restored
## Evolution of CSI-2 Imaging Interface

<table>
<thead>
<tr>
<th>Imaging Interface</th>
<th>Description</th>
<th>Release / Adoption</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Gen 1</strong></td>
<td><strong>CSI-2 v1.1</strong> protocol over D-PHY v1.1 (at 1.5 Gbps), and bidirectional command over I2C_FM (at 400 Kbps)</td>
<td>EOY 2012</td>
</tr>
<tr>
<td></td>
<td>Provides effective (usable) BW of 3 Gbps over 6 D-PHY v1.1 pins</td>
<td></td>
</tr>
<tr>
<td><strong>Gen 2</strong></td>
<td><strong>CSI-2 v1.2</strong> protocol over D-PHY v1.2 (at 2.5 Gbps), and bidirectional command over I2C_FM (at 400 Kbps)</td>
<td>EOY 2014</td>
</tr>
<tr>
<td></td>
<td><strong>CSI-2 v1.3</strong> protocol over C-PHY v1.0 (2.5 Gsps or 5.7 Gbps) and D-PHY v1.2 (at 2.5 Gbps), and bidirectional command over I2C_FM (at 400 Kbps)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Provides effective (usable) BW of 5 Gbps over 6 D-PHY v1.2 pins</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Provides effective (usable) BW of 11.43 Gbps over 6 C-PHY v1.0 pins</td>
<td></td>
</tr>
<tr>
<td><strong>Gen 3</strong></td>
<td><strong>CSI-2 v2.0</strong> protocol supports C-PHY v1.2 and D-PHY v2.1, with bidirectional command over I2C_FMP (1GHz) and I3C v1.0.</td>
<td>EOY 2016</td>
</tr>
<tr>
<td></td>
<td><strong>C-PHY v1.2</strong> provides up to 4.5 Gsps (10.3 Gbps) over 3 pins</td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>D-PHY v2.1</strong> provides up to 4.5 Gbps over 4 pins</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Bidirectional CCI over I2C_FMP provides around 880 Kbps of effective BW, and CCI over I3C v1.0 provides effective BW of: 10.67 Mbps over SDR, 19.2 Mbps over HDR-DDR, 18 Mbps over HDR-TSL, and 29.3 Mbps over HDR-TSP.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Provides effective (usable) BW of 9 Gbps over 6 D-PHY v2.1 pins</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Provides effective (usable) BW of 20.6 Gbps over 6 C-PHY v1.2 pins</td>
<td></td>
</tr>
</tbody>
</table>
CSI-2 over C-PHY PSD emission reduction from scrambling
CSI-2 over D-PHY PSD emission reduction from scrambling
CSI-2 Latency Reduction Transport Efficiency

- Reduce latency and improve efficiency (preserving PHY based delimiters / B2B)
- Provides longer reach over C/D-PHYs without need for redrivers or retimers
- Alleviates electrical overstress current leakages impediments
CSI-2 Sensor Fusion using CCI

Effective (usable) BW: 5 Gbps
Gross BW: 5 Gbps
Channel Rate: 2.5 Gbps

Effective (usable) BW: 11.4 Gbps
Gross BW: 11.4 Gbps
Channel Rate: 2.5 Gbps
CSI-2 CCI and AON Advancements 1/2

- Optimal pathway for multiple forward-looking advancements in imaging
  - Drivers: Health, Convenience, Security, Lifestyle, Efficiency
  - High-perf pixel conduit needs met with C/D-PHY advancements
  - Broad definitions and fuzzy range: (i.e. Wearable: Near Body, On Body, In Body)
  - Define imaging requirements for CCI, emerging AOI, array, and non-symmetrical applications

- Camera Controller Interface (CCI) and AON advancement considerations using I2C / I3C (SDR DDR, TSL, TSP)
  - Point-to-Point and Multi-Drop configurations
CSI-2 over C-PHY Virtual Channel Extension

5-bit Reserved Field (RES) + 3-bit Virtual Channel Extension (VCX) bit:
RES (bits 7:3) is set to zero and reserved for future use.
VCX (bit 2:0) is the most significant bits of the 5-bit Virtual Channel Identifier for the C-PHY Physical Layer option.

8-bit DATA IDENTIFIER (DI):
Contains the 2-bit Virtual Channel (VC) and the 6-bit Data Type (DT) Information.
VC (bits 7:6) is the least significant two bits of the 3-bit Virtual Channel Identifier. DT (bits 5:0) denotes the format/content of the Application Specific Payload Data. Used by the application specific layer.

16-bit WORD COUNT (WC):
The receiver reads the next WC 8-bit data words following the Packet Header.
The receiver uses the WC value to determine the end of the Packet Payload.

16-bit Cyclic Redundancy Check Code (PH-CRC):
16-bit CRC code for the Packet Header, computed over the Reserved, Data ID, and Word Count fields (4 bytes). Enables multi-bit errors to be detected.

CSI-2 *Insert Sync Word* PPI Command:
The physical layer simultaneously inserts a Sync Word on all N Lanes at this point as a result of executing a CSI-2 PPI command.

16-Bit Packet Data CRC:
Computed over WC Packet Data Words
Set to 00'
Set to 00''

PACKET HEADER (PH): 6N x 16-bits
(N = Physical Layer Lane Count)

PACKET DATA:
Length = Word Count (WC) * Data Word Width (8-bits). There are NO restrictions on the values of the data words

16-bit PACKET FOOTER (PF):
FC 8-bit bytes added to ensure that all Lanes transport the same number of 16-bit words; FC may be 0.
CSI-2 over D-PHY Virtual Channel Extension

8-bit DATA IDENTIFIER (DI):
Contains the 2-bit Virtual Channel (VC) and the 6-bit Data Type (DT) Information. VC (bits 7:6) is the least significant two bits of the 3-bit Virtual Channel Identifier. DT (bits 5:0) denotes the format/content of the Application Specific Payload Data. Used by the application specific layer.

16-bit WORD COUNT (WC):
The receiver reads the next WC data words independent of their values. The receiver is NOT looking for any embedded sync sequences within the payload data. The receiver uses the WC value to determine the end of the Packet Payload.

6-bit Error Correction Code (ECC) + 2 Virtual Channel Extension (VCX) bits
ECC (bits 5:0) enables 1-bit errors within the packet header to be corrected and 2-bit errors to be detected. VCX (bits 7:6) are the most significant bit of the 4-bit Virtual Channel Identifier for the D-PHY physical layer option.

APPLICATION SPECIFIC PAYLOAD

CHECKSUM/CRC (CS)

32-bit PACKET HEADER (PH)

PACKET DATA:
Length = Word Count (WC) * Data Word Width (8-bits). There are NO restrictions on the values of the data words

16-bit PACKET FOOTER (PF)
CSI-2 DPCM & HDR Advancements

• DPCM 12-10-12
  – SNR & IQ Benefits over varying degrees of noise, edges, MTF
  – Superior to straight RAW-10 capture or existing DPCM 12-8-12
CSI-2 HDR Advancements

- **HDR-16**

  - Data
  - Byte Values Transmitted LS Bit First

- **HDR-20**
Questions?
Backup
## MIPI C/D/M PHYs

### PHY Characteristics

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>M-PHY v3.1</th>
<th>D-PHY v1.2</th>
<th>C-PHY v1.0</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Primary use case</strong></td>
<td>Performance driven, bidirectional packet/network oriented interface</td>
<td>Efficient unidirectional streaming interface, with low speed in-band reverse channel</td>
<td>Efficient unidirectional streaming interface, with low speed in-band reverse channel</td>
</tr>
<tr>
<td><strong>HS clocking method</strong></td>
<td>Embedded Clock</td>
<td>DDR Source-Sync Clock</td>
<td>Embedded Clock</td>
</tr>
<tr>
<td><strong>Channel compensation</strong></td>
<td>Equalization</td>
<td>Data skew control relative to clock</td>
<td>Encoding to reduce data toggle rate</td>
</tr>
<tr>
<td><strong>Minimum configuration and pins</strong></td>
<td>1 lane per direction, dual-simplex, 2 pins each (4 total)</td>
<td>1 lane plus clock, simplex, 4 pins</td>
<td>1 lane (trio), simplex, 3 pins</td>
</tr>
<tr>
<td><strong>Maximum transmitter swing amplitude</strong></td>
<td>SA: 250mV (peak) LA: 500mV (peak)</td>
<td>LP: 1300mV (peak) HS: 360mV (peak)</td>
<td>LP: 1300mV (peak) HS: 425mV (peak)</td>
</tr>
<tr>
<td><strong>Data rate per lane (HS)</strong></td>
<td>HS-G1: 1.25, 1.45 Gb/s HS-G2: 2.5, 2.9 Gb/s HS-G3: 5.0, 5.8 Gb/s (Line rates are 8b10b encoded)</td>
<td>80 Mbps to ~2.5 Gbps (aggregate)</td>
<td>80Msym/s to 2.5 Gsym/s times 2.28 bits/sym, or max 5.7 Gbps (aggregate)</td>
</tr>
<tr>
<td><strong>Data rate per lane (LS)</strong></td>
<td>10kbps – 600 Mbps</td>
<td>&lt; 10 Mbps</td>
<td>&lt; 10 Mbps</td>
</tr>
<tr>
<td><strong>Bandwidth per Port (3 or 4 lanes)</strong></td>
<td>~ 4.0 – 18.6 Gb/s (aggregate BW)</td>
<td>Max ~10 Gbps per 4-lane port (aggregate)</td>
<td>Max ~ 17.1 Gbps per 3-lane port (aggregate)</td>
</tr>
<tr>
<td><strong>Typical pins per Port (3 or 4 lanes)</strong></td>
<td>10 (4 lanes TX, 1 lane RX)</td>
<td>10 (4 lanes, 1 lane clock)</td>
<td>9 (3 lanes)</td>
</tr>
</tbody>
</table>
CSI-2 over D-PHY signaling
CSI-2 over C-PHY (N-Phase) signaling

Detail of Programmable Sequence

Preamble
- Preamble is composed of: 3,3,3,3,..., with mid-section consisting of a programmable sequence.
- Reset initializes all to 3,3,3,3,...

Sync Word
- Sync Word: 3,4,4,4,4,4,3 (Least Significant Symbol first)

Packet Data
- Post is composed of multiple of unused code word: 4,4,4,4,4,4

LP-111 LP-001 LP-000