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New Trends in the High-Volume Manufacturing Test of MIPI-Based Devices
Agenda

• Introduction
• Hardware Requirements for MIPI Testing in Production
• Protocol Requirements for MIPI Testing in Production
• System-Oriented Testing & Case Studies
Typical Device Classes

(a) MIPI CSI-2™ 4-Lane
(b) MIPI CSI-2™ 4-Lane
(c) MIPI DSI-2™ 4-Lane
(d) MIPI DSI-2™ 4-Lane

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Test Methodology Spectrum

ATE or Bench Instrument Add-On (e.g. Scope) → Reduce Cost / Increase Quality → Test Module

Test Methodology Spectrum

Golden Device Methodology → Achieve Instrument Grade

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Test Methodology Spectrum – On-Board Channel Card

- Protocol Exerciser Fabric
- PHY
- Protocol Tester Fabric

Generate or detect MIPI-compliant signals and perform go/no-go testing.
Hardware Requirements
Low-Power (LP) and High-Speed (HS) Signaling

“High” LVCMOS* level
Used for low power mode

Up to 6x smaller amplitude
Up to 225x faster bandwidth

*LVCMOS = Low-Voltage Complementary Metal Oxide Semiconductor Logic
Switching Challenges on ATE

**Integrated Driver**

- With Hi-Z load
- Switch timing & charge injection cause poor timing control
- Proper D-PHY LP/HS transition
- Proper C-PHY LP/HS transition

**Conventional Switch-Based Solution**

- With Hi-Z load
- Challenges exist because of receiver switchable termination as well
Multi-Level HS Drivers and Comparators
Equalization Waveforms

**D-PHY**

![D-PHY Waveform Diagram](image1)

**C-PHY**

![C-PHY Waveform Diagram](image2)
Bidirectional Bus Control

Tester Driving
Device Under Test (DUT) Driving
Tester Driving
Protocol Requirements
Packet Based Communication

Build packet as list of bytes

Header
- Data Identifier
- Wordcount (lsb/byte)
- Wordcount (msb/byte)
- EEC

Payload
- Payload byte 0
- Payload byte 1
- Payload byte 2
- Payload byte 3
- Payload byte 4
- Payload byte 5

Footer
- Payload CRC (lsb/byte)
- Payload CRC (msb/byte)

Bytes

Preparation for HS Data
Start of HS
HS Data (Packet Transmission)
End of HS

Low Power State

Low Power State
DUT Configuration Through the MIPI Bus

Real Display Driver IC Programming Sequence
Functional Testing on ATE

**Protocol-Based Test Solution**

Start-up commands are programmed through the integrated driver without requiring ATE vectors.

**Conventional Switch-Based Solution**

Cumbersome nature of ATE vectors often forces test engineers to choose very limited test coverage.
System-Oriented Testing and Case Studies
Microcontroller CSI-2 Input Test

1. ATE commands module to begin test
2. Test module begins MIPI D-PHY transmission
3. ECC/CRC result sent to Test Module or ATE for comparison and pass/fail

Single Timing Cycle Required From ATE
Microcontroller CSI-2 Input Test

- ATE to Test Module
- Set Voltage
- Start Transmission
- Test Module MIPI Output
- MIPI Test Pattern

Images:
- Slow control words
- High-speed test data
DDIC* with Integrated Device Response Checking

*DDIC = Display Driver IC
Image Sensor Test

Module used as a fast capture tool

Low-Speed ATE with Image Processor

Illuminator

DUT
Summary

- Increasing requirements have emerged for at-speed testing of MIPI-based devices
- System-like solutions are being developed by manufacturers of microcontrollers, image sensors, display drivers, and storage devices
- Hardware and protocol requirements for enabling the test of such solutions have been described in this presentation
ADDITIONAL RESOURCES

- [https://introspect.ca/](https://introspect.ca/) – Total solutions for most high-speed interface technologies
THANK YOU