Outline

• Introduction to MIPI I3C℠
• Usages beyond sensing
  – MIPI Camera Control Interface (CCI℠)
  – MIPI Touch over I3C℠
  – MIPI Debug for I3C℠
• MIPI I3C℠ feature descriptions
• Implementation guidelines
  – Legacy Device Support
  – HDR Modes
  – Varied Topologies
• Summarized good design practices
MIPI I3C℠ for Ubiquitous Low Speed Interfacing

• Anywhere sensors are used, MIPI I3C℠ belongs
• Aimed toward historical I²C, SPI and UART applications in…
What is MIPI I3C℠?

• Innovative new 2-Wire Sensor interface
• Key features address historical pain points
  – In-band Interrupt, Dynamic Addressing, Multi-Master, Standardized Commands, Time Control, Hot-Join, Error Detection and Recovery
  – Plus...
  
  - PC Compatibility
  - Low Power
  - High Data Rates

[Graph showing energy consumption and data rates for I3C vs. I2C]

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MIPI I3C<sup>SM</sup> Vision?

- I²C Compatibility
- In-band Interrupt
- Common Command Codes
- Reduced Signal Count
- Reduced Interface Power

Too Many I/Os! Fragmented Interfaces!
Usages Beyond Sensing

- MIPI CCI\textsuperscript{SM} (Camera Control Interface) over I3C\textsuperscript{SM} offers faster, lower latency and more efficient camera control with future abilities to support grouped data write and AON imaging.

- Current touch screen controller interfaces are fragmented.
- For many touch screens, MIPI Touch over I3C\textsuperscript{SM} presents a converged interface option for processed and raw touch data, leveraging IBI and HDR modes.

- MIPI Debug for I3C\textsuperscript{SM} offers a more complete closed chassis, scalable and power aware platform debug capability with minimum boundary pin count.
MIPI I3C℠ Features

- **I3C SDR – The Base Interface**
  - Up to 12.5 MHz $I^2C$-like clocking with defined Open-Drain / Push-Pull
  - Supports multiple classes of Devices
    - I3C Main Master
      - SDR-only Main Master
    - I3C Secondary Master
      - SDR-Only Secondary Master
    - I3C Slave
      - SDR-Only Slave
    - $I^2C$ slave
MIPI I3C℠ Features

• **SDR Dynamic Address Assignment**
  - Standardized procedure for dynamic assignment of 7-bit Addresses to all I3C Devices
    - I3C Slaves have two standardized characteristics registers and an internal 48-bit Provisional ID to aide the procedure
  - Legacy I²C Devices still use their static I²C Address

• **SDR In-band Interrupt**
  - Slave device can issue START Request when in “Bus Available” state
  - Master provides Interface Clock for Slave to drive it’s Master-assigned address onto the bus
  - Lowest assigned address wins arbitration in Open-Drain configuration
  - A data payload (i.e. Mandatory Data Byte) can immediately accompany the In-band Interrupt
# MIPI I3C Features

- **Error Detection and Recovery Methodology**
  - For Master and Slave generated errors (9 Error Types identified, Parity, CRC5)

- **Common Command Codes**
  - Standardized command mode with extensible set of MIPI-defined codes that can be Broadcasted and/or Directed, Read and/or Write

<table>
<thead>
<tr>
<th>S or Sr</th>
<th>0x7E / W / ACK</th>
<th>Command Code / T</th>
<th>Data (Optional) (Broadcast CCC only) / T</th>
<th>Sr or P</th>
</tr>
</thead>
</table>

- **Standardized Command Codes**
  - Event Enable/Disable
  - Activity States
  - Payload Mgmt
  - I3C Feature Mgmt (Dynamic Address Assignment, Mastership, HDR Modes, Timing Control)
  - Test Modes
  - Extensible Space (MIPI and Vendor)

* Example of Broadcast CCC Frame
Guidelines - Legacy I²C Device Support

- Fm and Fm+ Speeds Supported
- 50ns Spike Filter ($t_{SP}$) Needed for 12.5MHz I3C<sup>SM</sup> Clocking

Clock Stretching is Not Allowed – I3C SCL is Push/Pull
- 20mA Open Drain Drivers ($I_{OL}$) are Not Used
- I²C Extended Addresses (10 bit) are Not Used

$t_{SP}$: pulse width of spikes that must be suppressed by the input filter

*UM10204: I2C-bus specification and user manual Rev. 6
MIPI I3C<sup>SM</sup> Features

- **I3C High Data Rate (HDR) Modes**
  - Optionally supported beyond the base SDR mode: 12.5MHz, SDA/SCL
    - HDR-DDR: Double Data Rate
    - HDR-TSL/TSP: Ternary Symbol
  - Offer bit rates over 33Mbps at a fraction of the per bit power of I<sup>2</sup>C Fast Mode
  - Simple Slave-side digital implementations
  - Coexistent with legacy I<sup>2</sup>C Devices
  - Leverage rising and falling edges
  - Individually entered using broadcasted MIPI-defined Common Command Codes
  - Universally exited and restarted via MIPI-defined toggling patterns
    - Allows non-HDR I3C Devices to “ignore” HDR transmissions

<table>
<thead>
<tr>
<th>I3C</th>
<th>Msg1</th>
<th>Msg2</th>
<th>I3C</th>
</tr>
</thead>
<tbody>
<tr>
<td>START</td>
<td>Brcst CCC</td>
<td>EnterHDRx</td>
<td>HDR Exit Pattern</td>
</tr>
<tr>
<td></td>
<td>Setup (SDA/SCL)</td>
<td>End (if needed)</td>
<td>HDR Reset Pattern</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>HDR Cmd</td>
</tr>
<tr>
<td>SDA</td>
<td></td>
<td></td>
<td>HDR Exit</td>
</tr>
<tr>
<td>(Exit)</td>
<td></td>
<td></td>
<td>Pattern</td>
</tr>
<tr>
<td>SCL</td>
<td></td>
<td></td>
<td>HDR Restart</td>
</tr>
</tbody>
</table>

![Diagram](image-url)
MIPI I3C<sup>SM</sup> Features

- **HDR-DDR: Double Data Rate**
  - Uses SCL as a clock, however Data and Commands change SDA on both SCL edges. By contrast, SDR Mode changes SDA only when SCL is Low
  - HDR-DDR moves data by Words, which generally contains 2 preamble bits, 2 payload bytes and 2 parity bits. 4 Word Types defined: Command, Data, CRC, and Reserved

- Simple protocol:

  - **S or Sr**
    - DC Reserved byte (0x7E) (0x80) =
  - **ACK**
    - Enter HDR-DDR
    - CRC (ENTHDR)
  - **T**
    - HDR-DDR Command
    - HDR-DDR Data (1 or more words)
  - **P**
    - HDR-DDR CRC
    - HDR RESTART

  From Master to Slave
  - ACK = Acknowledge (SDA Low)
  - NACK = Not Acknowledge (NACK)
  - S = START Condition
  - Sr = RESTART Condition
  - P = STOP Condition
  - T = Transition Bit Alternative to ACK/NACK

  From Slave to Master
  - Transition Bit (Parity Bit for CCC)

  Parity Bits
  - P1: Odd parity bit
  - P0: Even parity bit

  Command, Data, or CRC
  - Based on Preamble (2-bit MSB)
MIPI I3C\textsuperscript{SM} Features

- **HDR-TSL/TSP: Ternary Symbol Coding**
  - Ternary symbol coding for pure (TSP) and I\textsuperscript{2}C legacy-inclusive (TSL) systems
  - Given a two-wire interface with ‘simultaneous’ transitions and no traditional clock, there are 3 possible symbols available – 0, 1, 2

- At least one line must transition each period
- Ideally, there are 3 possible “next” transition
- Transition indices are used to efficiently encode Binary into Ternary
- Simple protocol:

<table>
<thead>
<tr>
<th>HDR-TSL/TSP</th>
<th>SDA</th>
<th>SCL</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>00</td>
<td>01</td>
</tr>
<tr>
<td>10</td>
<td>11</td>
<td>01</td>
</tr>
<tr>
<td>00</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
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<tr>
<th>HDR-TSL/TSP</th>
<th>SDA</th>
<th>SCL</th>
</tr>
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<tbody>
<tr>
<td>One symbol</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>\textsuperscript{i\textsubscript{2}}C and I3C SDR</th>
<th>SDA</th>
<th>SCL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data line stable; data valid</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Change of data allowed</td>
<td></td>
<td></td>
</tr>
</tbody>
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<td>START</td>
<td>Brdcst CCC EnterHDRx HDR Cmd HDR Data HDR Restart Pattern HDR Cmd HDR Data HDR Exit Pattern STOP</td>
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Guidelines - HDR Modes

- Enter HDR Commands Supported

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<td>HDR Data</td>
<td>HDR Exit Pattern</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HDR Data</td>
<td>HDR Data</td>
<td>STOP</td>
</tr>
</tbody>
</table>

- HDR Exit Pattern detected by all I3C Devices

- Non-HDR Devices shall ignore I3C HDR bus traffic until the HDR Exit Pattern is detected
Guidelines - Varied Topologies

- Impacts on signal transition/transit times (maximum bus frequency)
  - SDA/SCL drive strength: “weaker” for lower power and interference vs “stronger” for faster over larger topologies/loads
  - Trace length and material: short vs long and pcb vs cable
  - SCL/SDA pad capacitance
  - Clock to Data Turnaround Time ($t_{SCO}$)

- Legacy $I^2C$ Devices impact maximum bus frequency (MHz)
  - Must run $I^2C$ at speeds/pulses beyond Spike Filter or slow Bus to that of slowest $I^2C$ Device

- Impacts on signal integrity/reliability
  - Device Location: close and far Devices can cause interference from reflections
Summarized Good Design Practices

• Thoroughly understand capability of coexistent Legacy I\(^2\)C Devices
  – 50ns Spike Filter
  – Disabled Clock Stretch

• Understand bus topology and performance tradeoffs Mixed (I\(^3\)C and Legacy I\(^2\)C Devices) vs Pure Bus (I\(^3\)C Devices Only)
  – Trace length and material
  – SDA/SCL pad capacitance
  – Clock to Data Turnaround Time (t\(_{SCO}\))
  – Device location
Any Questions?