MIPI C-PHY\textsuperscript{SM} And How It Enables Next Generation Display and Camera Implementations
Original Spark: Three Phase Encoding!

1 Unit Interval of Data

2.285 Bits of Information

George Wiley, Qualcomm
Basic Concept – One Trio

Single-Ended Field of Transmitters

Differential Field of Receivers

A

B

C

AB

BC

CA
Three Voltage Levels Ensure Proper Differential Reception

A  B  C

Both A and B dip together, but receiver still sees a logic 1

Regular Binary Receiver!
Always-Toggle Design Allows for Simple Clock Recovery (100% Aggregate Transition Density)

Single-Ended Field of Transmitters

Differential Field of Receivers
Key Takeaways

Three-level single-ended signaling

Non-deterministic transitions based on self-clocked mapping and encoding algorithm
Encoding and Mapping
MIPI CPHY™ Data Types

**ANALOG**

- 3 wires per lane
- 3-level wires (LOW, MID, HIGH)
- Every unit interval must contain LOW, MID, and HIGH wires
- No two consecutive identical states

**DIGITAL**

- Wire differential
- Wire States (3 bits)
- Symbols (3 bits)
- Integers (16 bits)

Symbols (3 bits):

- A > B
- B > C
- C > A

Integers (16 bits):

- 0x7290
## Wire States

- A wire state is the collection of A, B, and C
- 6 possible wire states

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>A&gt;B</th>
<th>B&gt;C</th>
<th>C&gt;A</th>
<th>Wire state name</th>
</tr>
</thead>
<tbody>
<tr>
<td>HIGH</td>
<td>LOW</td>
<td>MID</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>+x</td>
</tr>
<tr>
<td>LOW</td>
<td>HIGH</td>
<td>MID</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>-x</td>
</tr>
<tr>
<td>MID</td>
<td>HIGH</td>
<td>LOW</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>+y</td>
</tr>
<tr>
<td>MID</td>
<td>LOW</td>
<td>HIGH</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>-y</td>
</tr>
<tr>
<td>LOW</td>
<td>MID</td>
<td>HIGH</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>+z</td>
</tr>
<tr>
<td>HIGH</td>
<td>MID</td>
<td>LOW</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>-z</td>
</tr>
</tbody>
</table>
Symbols: Now We’re Transmitting!

- A symbol represents a transition between two wire states
- 5 possible symbols

<table>
<thead>
<tr>
<th>Symbol (3 bits)</th>
<th>Flip</th>
<th>Rotate</th>
<th>Polarity</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>DC</td>
<td>DC</td>
</tr>
</tbody>
</table>

**Flip**
- 0: -
- 1: Same letter, toggle sign.

**Rotate**
- 0: Decr. letter
- 1: Incr. letter

**Polarity**
- 0: -
- 1: Toggle sign

Example:

- $+x \rightarrow 1 \rightarrow -z$
- $-z \rightarrow 3 \rightarrow +x$
MIPI C-PHY℠ defines a mapping between 7-symbol words and 16-bit integers.

Number of 7-symbol words: $5^7 = 78125$

Number of 16-bit integers: $2^{16} = 65536$

- 65536 7-symbol words
- 12589 unmapped words
- 0x7290 65536 16-bit integers
Global Packet Transmission Similar to MIPI D-PHY\textsuperscript{SM}

<table>
<thead>
<tr>
<th>D-PHY\textsuperscript{SM}</th>
<th>C-PHY\textsuperscript{SM}</th>
</tr>
</thead>
<tbody>
<tr>
<td>LP-11</td>
<td>LP-01</td>
</tr>
<tr>
<td><strong>HS-ZERO</strong></td>
<td><strong>SoT</strong></td>
</tr>
<tr>
<td>0 0 0 0 0 0 ... 0 0</td>
<td>0 0 0 1 1 1 0 1</td>
</tr>
<tr>
<td><strong>T3-PREBEGIN</strong></td>
<td><strong>SYNC</strong></td>
</tr>
<tr>
<td>3 3 3 3 3 3 3 3</td>
<td>3 4 4 4 4 4 4 4</td>
</tr>
</tbody>
</table>

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Tool View

Three-Phase Signals

Decoded Data
MIPI C-PHY’s Magical Unmapped Words!
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- 65536 16-bit integers
- 12589 unmapped words

- Sync Word (Alignment marker) $\{3444443\}$
- Post (End-of-Packet marker) $\{4444444\}$
Easily Delineate Bursts... Really Easily!

SYNC and POST

Unmapped Word (SYNC START OF TRANSMISSION MARKER)

Unmapped Word (POST END OF TRANSMISSION MARKER)
Send Unmapped Words Within HS Bursts!
Example: Packet Header Resynchronization

MIPI CSI-2™ Packet

Bytes

Reserved Data Identifier Wordcount (lsbyte) Wordcount (msbyte) CRC (lsbyte) CRC (msbyte) Reserved Data Identifier Wordcount (lsbyte) Wordcount (msbyte) CRC (lsbyte) CRC (msbyte)

0x00 0x24 0x80 0x07 0x08 0x9B 0x00 0x00 0x00 0x00 0x01 0x02 0x03 0x04 0x05

Invisible in Integer Domain, But Transmitted in Symbols!
Example: Alternate Low Power Mode

Frozen Wire State

ALP PAUSE STOP  ALP PAUSE WAKE
Example: Alternate Low Power Mode

STOP
EME
LPDT COMMAND
LPDT BYTE
ALP PAUSE STOP
ALP PAUSE WAKE
PREAMBLE
LPDT START
LPDT NIBBLE

Unmapped Word
Unmapped Word
### Unmapped Words Enable a Wide Range of Codes

<table>
<thead>
<tr>
<th>Symbol Sequence</th>
<th>ALP Function Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>02444440</td>
<td>Stop Code</td>
</tr>
<tr>
<td>02444441</td>
<td>ULPS Code</td>
</tr>
<tr>
<td>02444442</td>
<td>Trig 1 Code</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>44444444</td>
<td>Post2</td>
</tr>
</tbody>
</table>

*Same functionality as legacy LP EME Sequences*
Multiple SYNC Word Types
SYNC Is an Unmapped Word

• Five (5) possible SYNC words exist
  – 3444440
  – 3444441
  – ...

• First SYNC word in a burst is always 3444443

• Multiple SYNC words used to trigger different seed types for MIPI CSI-2 SM scrambling
MIPI CSI-2\textsuperscript{SM} Imaging Features Enabled by C-PHY
Effective (usable) BW: 11.4 Gbps

Gross BW: 11.4 Gbps
Channel Rate: 2.5 Gsps

12C Compatible 2-wire Camera Control

Src: MIPI Alliance
MIPI CSI-2\textsuperscript{SM} Imaging Features Enabled by MIPI C-PHY\textsuperscript{SM}

- **Long Reach Transport Efficiency (LRTE)**
  - Easily delimits packets using *unmapped words*
- **ALPS**
  - Helps maintain low voltage levels in advanced process nodes
- **Up to 32 Virtual Channels**
  - Useful for imaging and vision applications supporting *multiple sensor streams*
MIPI CSI-2\textsuperscript{SM} Imaging Features Enabled by MIPI C-PHY\textsuperscript{SM}

• Scrambling
  – Provides a \textit{wide range of seed} triggers using multiple SYNC words

• Future support for sensor fusion and camera commands
  – MIPI C-PHY\textsuperscript{SM} natively enables future technologies for more efficient camera commands than those using legacy LP mode
MIPI DSI-2$^\text{SM}$ Protocol Features
Enabled by MIPI C-PHY$^\text{SM}$
MIPI DSI-2℠ Features Enabled by MIPI C-PHY℠

- Fast packets
  - Unmapped words enable very robust packet delimiting within a burst

```
Packet i
  No Ambiguity

Packet i+1
```
MIPI DSI-2℠ Features Enabled by MIPI C-PHY℠

- Display stream compression
  - Complete compatibility with compression needs

Original image: 24 BPP  
On the wire: 8 BPP  
Received image: 24 BPP
MIPI DSI-2\textsuperscript{SM} Features Enabled by MIPI C-PHY\textsuperscript{SM}

- MIPI Display Command Set (DCS\textsuperscript{SM}) Mode
  - Proven technology for buffered frame transmissions
- Scrambling
  - Full support for scrambling at the protocol level
Summary

MIPI C-PHY\textsuperscript{SM} is based on a three-phase encoding scheme resulting in high transport efficiency over bandwidth-constrained channels.

MIPI C-PHY\textsuperscript{SM}’s unmapped words create extremely robust control, transmission, and messaging mechanisms at the protocol level.

Next generation imaging (MIPI CSI-2\textsuperscript{SM}), vision (MIPI CSI-2\textsuperscript{SM}), and projection (MIPI DSI-2\textsuperscript{SM}) applications can benefit greatly from MIPI C-PHY\textsuperscript{SM}’s powerful protocol features.