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Next Generation MIPI Physical Layer Design and Evaluation Challenges
Agenda

• New specification and CTS changes in 2017
• Eye diagram tests changes and challenges
  – MIPI C-PHY\textsuperscript{SM}
  – MIPI D-PHY\textsuperscript{SM}
  – MIPI M-PHY\textsuperscript{®}
• SSC test
  – MIPI D-PHY\textsuperscript{SM}
Specification updates in MIPI C-PHY

- TX Pre-Emphasis(TxEQ option) – from Pre-emphasis method to de-emphasis method
- RCLK jitter(reference clock jitter) – Annex to chapter 9
- Receiver calibration – removing PVT(Process, Voltage and Temperature variation after Long LP signal)
CTS updates in MIPI C-PHY

- Test 1.2.21 – Tx Eye Pattern Test
- Test 1.4.1 – HS-TX Differential Voltages Unterminated
- Test 1.4.2 – HS-TX Differential Voltage Mismatch Unterminated
- Test 1.4.3 – HS-TX Single-Ended Output High Voltages Unterminated
- Test 1.4.4 – HS-TX Static Common-Point Voltages Unterminated

CTS 1.0: Approved Feb 12, 2016
CTE 1.1: Expected approve Aug, 2017
Specification updates in MIPI D-PHY

- Up to 6500Mbps with Short reference channel (8K support)
- Lower LP voltage level from 1.2V to 1V
- HS-Idle (lower latency)
- Programmable Preamble (RX PVT calibration due to LP signal)

D-PHY 2.0 : Approved Mar 8, 2016
D-PHY 2.1 : Approved Mar 28, 2017
CTS updates in MIPI D-PHY

- Test 1.5.7 – HS-TX Eye Diagram
- Test 1.4.19 – TX Spread Spectrum Clocking (SSC) Requirement
- ZID open case test
- Direct connection supporting in HS continuous mode.

CTS 1.2: April 24, 2017

CTS v2.0/v2.1

CTS 2.0/2.1: expected finished in October
Specification updates in MIPI M-PHY

- Minor spec clarification
- Target BER $10^{-10}$ to $10^{-12}$

M-PHY 4.0 : Approved Aug 3, 2015

M-PHY 4.2.1 : Approved Mar 28, 2017
CTS updates in MIPI M-PHY

- **CTS 3.1**: On-going (revision 21)
  - Test 1.1.7 – HS-TX G3 and G4 Differential AC Eye (TEYE-HS-G3/G4-TX, VDIF-AC-HS-G3/G4-TX)

- **CTS 4.0/4.1**: On-going (revision 1)
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Eye Diagram Test - General

MIPI C-PHY

MIPI D-PHY

MIPI M-PHY

Reference channel

Figure 26 HS-G3 and HS-G4 Reference Channel Insertion Loss XED L was used in the templates.
Eye Diagram Test Challenges for MIPI C-PHY/D-PHY

- RTB (Reference Termination Board) can’t support new specifications

Same data, +/-250mV HS swing, 82ps R/F time, without reference channel
However, eye diagram is distorted
Now, PHY WG defines direct connection to oscilloscope

However, RTB is still required for LP to HS timing test.
Resolving Issue with Direct Connection

- Direct connection provides more accurate results on tests.

<table>
<thead>
<tr>
<th>Speed (Gsps)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>500M</td>
<td>Same data, +/-250mV HS swing, 82ps R/F time, without reference channel</td>
</tr>
<tr>
<td>1G</td>
<td></td>
</tr>
<tr>
<td>1.5G</td>
<td></td>
</tr>
<tr>
<td>2.0G</td>
<td></td>
</tr>
<tr>
<td>2.5G</td>
<td></td>
</tr>
</tbody>
</table>

sps: Symbol Per Second
Chip Design Tip for Testing

- New MIPI C-PHY v1.1 and D-PHY v2.0 or above require to send both Burst mode and Continuous mode signal on testing, so it is good to consider to implement both mode for easy testing.
- If not, it is not easy to get right test result.

**MIPI C-PHY CTS Annex B**

- Notes on the above Test Setup #2:
  - The DUT is connected to the DSO using three high-bandwidth, low loss 50-ohm coaxial cables.
  - For tests where a reference channel is required, it can either be a physical channel or be implemented in software on the oscilloscope.
  - Each cable measures the single-ended V_A, V_B, or V_C signal with respect to PCB ground.
  - The DSO serves as the termination, and is designed to have a resistive termination (Zm/2) value of 50 ohms per line, for all lines. The DSO input coupling and/or termination voltage must be set appropriately for this configuration.
  - The DUT should be configured to transmit a continuous stream of HS data, because this test setup is suitable for measurements in the HS mode of operation.
  - The DSO vertical gain should be optimized so that the DUT signaling spans as much of the vertical height of the screen as possible.

**MIPI D-PHY CTS Annex B**

- Note on the above test setup #2:
  - The DUT is connected to the DSO using high-bandwidth, low loss 50O SMA cables.
  - For tests where a reference channel is required, it can either be a physical channel or be implemented in software on the oscilloscope.
  - Each cable connected to single-ended – or – signal with respect to PCB ground.
  - The DSO serves as the termination, and is designed to have a resistive termination(ZID/2) value of 50O per line, for all lines. The DSO input coupling and/or termination voltage must be set appropriately to emulate 100Ω terminations in real D-PHY.
  - The DUT should be configured to transmit a continuous stream of HS data only, because this test setup is suitable for measurements in the HS mode of operation with only 100Ω termination emulation.
  - The DSO vertical gain should be optimized so that the DUT signaling spans as much of the vertical height of the screen as possible.
Test Setup Tip 1

- Prepare Test Fixture (TVB) with short routing to connector to reducing fixture line loss (5cm or less) or extract S-parameter of fixture trace when design TVB
- To emulate 100ohm termination in MIPI PHY, please use external voltage sourced scope or probe to compensate common mode voltage drop and double current consumption
Test Setup Tip 2

- Use hardware or software channel for eye diagram test, all oscilloscope vendor provide easy tool for software channel embedding, using S-parameter file.
- For MIPI C-PHY and D-PHY, it requires more than 2 lines of channel so software embedding provide more price merit than real hardware channel, also convenient to test.
MIPI M-PHY Eye Diagram Test

- Test setup is same on both HSG3 and HSG4 but testing points has changed.
MIPI M-PHY Embedding Channel + Package Model

DUT

Gear3

CH1/CH2

PLL

Oscilloscope

Gear4

CH1/CH2

PKG

CTLE

PLL

DFE

-3dB at 5.83GHz
Test Setup Tip 3 – and Must for HS Gear4

- Reference package plus pad capacitance model is not real material for using, so it is hard to emulate with real PCB or another circuit, so MIPI WG recommends using software embedding function for embedding reference package plus pad capacitance model.
MIPI M PHY RX Equalizer-CTLE

• Not likely another application, M PHY CTLE has vary wide range of zero pole value and Adc value

What if A company think 2.5dB Adc + 400MHz Fz is optimal CTLE value

B company think 0dB Adc + 400MHz Fz is optimal CTLE value?

Does it correlated between?
MIPI M-PHY RX Equalizer-CTLE

Same waveform but only change Adc value from 2.5dB to 0dB

2.5dB Adc case
Fz = 400MHz

0dB Adc case
Fz = 400MHz

Adc : CTLE DC gain
Fz : CTLE zero frequency
MIPI M-PHY RX Equalizer-DFE

Also Oscilloscope’s DFE setting is not favor to the customer.
MIPI M-PHY RX Equalizer-DFE

Also Oscilloscope’s DFE setting is not favor to the customer.

Tap = $V_{DFE\_RX}/Amplitude$

Amplitude or upper/lower target is voltage value after CTLE applied. Not direct $V_{DFE\_RX}$ value
MIPI M-PHY RX Equalizer-DFE

$V_{\text{DEF,RX}}$: DFE feedback voltage signal

$40\text{mV} V_{\text{DEF,RX}}$

$40\text{mV}/133\text{mV} = 0.30075$

$60\text{mV} V_{\text{DEF,RX}}$

$60\text{mV}/133\text{mV} = 0.45112$
Test Setup Tip 4

Use SigTest tool

Commonly used for High speed digital interface
  • USB
  • PCIe

Provide similar result between oscilloscopes
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SSC (Spread Spectrum Clocking) - General

- SSC makes distribution of RF power on signal so that it can reduce interruption to another signals like wireless signal.
- Now MIPI D-PHY fundamental frequency is over 2GHz bandwidth, where lots of wireless signals have used.
- Because of Clock line in MIPI D-PHY, SSC feature is required.

- Peak power: -6dBm = 112mV
- Peak power: -22dBm = 17.8mV
SSC (Spread Spectrum Clocking) Test in MIPI D-PHY

- SSC modulation frequency
- SSC modulation deviation
- SSC df/dt
SSC in MIPI D-PHY Specification

### Table 39 Spread Spectrum Clocking Requirements

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Modulation Rate</td>
<td>T_{SSC_MOD_RATE}</td>
<td>30</td>
<td>33</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>SSC Deviation</td>
<td>T_{SSC_FREQ_DEV}</td>
<td>-5000</td>
<td>0</td>
<td>PPM</td>
<td>1, 2</td>
</tr>
<tr>
<td>SSC df/dt</td>
<td>SSC_{df/dt}</td>
<td>N/A</td>
<td>1250</td>
<td>PPM/μs</td>
<td>3, 4, 5</td>
</tr>
</tbody>
</table>

**Note:**

1. The required SSC deviation is also called “Down-Spread”.
2. Any implementation with an SSC deviation significantly smaller than 5000 PPM may fail in EMI testing below 1 GHz clock rate (Data Rate < 2 Gbps).
3. df/dt limit shall be for clock and all data lanes.
4. Measured over a 0.5 μs interval using an alternating 010101010... input pattern at highest data rate. The measurements shall be low pass filtered using a filter with 3 dB cutoff frequency that is 60 times the modulation rate. The filter stopband rejection shall be a second order low-pass of 40 dB per decade. Evaluation of the maximum df/dt is achieved by inspection of the low-pass filtered waveform.
5. Maximum change rate of 1250 PPM/μs is limiting the absolute value of the df/dt.
Chip Design Tip for Testing

• For SSC (spread spectrum clocking), Designer must implement Chip can enable and disable SSC transmission.

10.2.2 Normative Spread Spectrum Clocking (SSC)

Spread Spectrum Clocking (sometimes referred to as “Spectrum Spread Clocking”) is a common technique where a low frequency modulation is added to the Transmitter’s clock to reduce the peak emissions.

All Transmitters conformant to D-PHY v2.0 and above shall support SSC as per Table 39 for data rates operating above 2.5 Gbps.

All Receivers conformant to D-PHY v2.0 and above shall support SSC as per Table 39 for data rates operating above 2.5 Gbps.

All Transmitters conformant to D-PHY v2.0 and above shall provide the system integrator with a mechanism to enable/disable SSC transmissions.

SSC can be used in HS Data Transmission Mode. If used during HS Data Transmission Mode, SSC transmission shall be consistent during the entire mode.

SSC should not be used in Escape mode.

SSC shall be implemented within the Transmitter such that a single modulated profile, single modulation rate and a single SSC deviation is common between the clock and all High-speed data lanes.

All SSC parameters are defined for the HS Clock.
Test Setup Tip 5

Use 2\textsuperscript{nd} order Butterworth filter to meet SSC df/dt test condition

Some of Digital oscilloscope are possible to use Matlab code in the oscilloscope itself so that Matlab can apply complicated filter function.

Transfer function

\[ A(\omega) = \frac{G_0^2}{1 + \left(\frac{\omega}{\omega_0}\right)^n} \]

where
- \( n \) = order of filter
- \( \omega_0 \) = cutoff frequency (approximately the -3dB frequency)
- \( G_0 \) is the DC gain (gain at zero frequency)

2\textsuperscript{nd} order Butterworth filter

\( \omega_0 = \text{cutoff frequency} \)

\( = 40\text{dB/decade} \)
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