IO Aggregation/De-Aggregation in Mobile & Mobile Influenced Systems to Improve Routing Congestion
Agenda

• Mobile & mobile-influenced system evolution
  – Low-speed I/O proliferation and MIPI standardization efforts

• System-level challenges
  – Bus topologies (I\textsuperscript{2}C, SPI, MIPI-I\textsuperscript{3}C, MIPI-VGI, etc.)
  – Routing congestions

• Reducing wires
  – Aggregation / De-aggregation

• Summary
Mobile-Influenced: Multiple Modules

Multiple Control Busses and GPIOs – Low Speed Communications

Congested Inter-Modular Connectivity

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But, over time, it will add yet another bus to the mix

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• Summary

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Challenge: Different Protocols and Bandwidths

- **SPI**
  - 4 pin IF 10+ Mbps

- **I2C**
  - 2 pin IF @ 400KHz
  - 2 pin IF @ 100KHz
  - 2 pin IF @ 1000KHz

- **UART**
  - 2 pin IF

- **MIPI CSI2 CCI**
  - I2C like

- **MIPI I3C**
  - 2 pin IF @ 12.5MHz

- **GPIO**
  - Various

- **PDM**
  - 2 pin IF

- **MIPI SoundWire®**
  - 2 pin IF

- **I2S**
  - 2 pin IF

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System Architecture Trends: Routing Limitations

POGO Pin architecture

Module A

Module B

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FlexPCB architecture

Board A

Board B

1-2 layer
Issues Identified

- SOCs are minimizing the number of direct signal connections
- PCBs are becoming smaller which adds to routing complexity
- Signals need to be pre-conditioned prior to reaching the SOC
- Localized or pre-processing demands are increasing
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• Summary
Signal Aggregation / De-Aggregation

Low power
Low cost
Small size

FPGA
#1

Module or Board A

POGO Pins
Or
Flex Cable

FPGA
#2

Module or Board B

SPMI
SoundWire
SPI
SoundWireXL
I2C
UART
DSI
GPIO

SLVS
CSI-2
I3C
I2S
PDM
RFFE
SlimBus
SMBus/PMBus
GPIO

SLVS
CSI-2
I3C
I2S
PDM
RFFE
SlimBus
SMBus/PMBus
GPIO
Signal Aggregation / De-Aggregation

Low power  
Low cost  
Small size  
**FPGA**  
#1

Module or Board A

POGO Pins  
Or  
Flex Cable

~1-5 mW  
~2x2 mm2

Low power  
Low cost  
Small size  
**FPGA**  
#2

Module or Board B
How Does Aggregation in an FPGA Work?

50 Mbps Serialized Envelope

Time Division Multiplexing – Multiple Packets

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How Does Aggregation in an FPGA Work?

Packetized data across serialized interface

- Serialized CDR interface for easier board routing
- Signals transmitted via a packet-based structure
  - Improved data integrity (CRC, FEC, etc.), 8b/10b enc
- Transmitted using a clock tolerance compensation (CTC)
  - Allows difference in reference clocks on each end
- Buffered / conditioned prior to reaching SOC
- Pre-processed for always-on capability
- Bridged to an interface the SOC can understand (i.e., SPI, I3C)

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### Resources Used

<table>
<thead>
<tr>
<th>Block</th>
<th>Gates*</th>
<th>Registers</th>
<th>RAMs</th>
</tr>
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<tbody>
<tr>
<td>CDR Encoding</td>
<td>3,000</td>
<td>210</td>
<td>-</td>
</tr>
<tr>
<td>RX Protocol Logic</td>
<td>1,400</td>
<td>105</td>
<td>-</td>
</tr>
<tr>
<td>TX Protocol Logic</td>
<td>4,300</td>
<td>130</td>
<td>-</td>
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<tr>
<td>GPIO interface</td>
<td>300</td>
<td>50</td>
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<tr>
<td>I2C Local Slave interface</td>
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<td>165</td>
<td>-</td>
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<tr>
<td>I2S interface</td>
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<td>725</td>
<td>4</td>
</tr>
<tr>
<td>Other</td>
<td>100</td>
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<td>-</td>
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<tr>
<td><strong>TOTAL</strong></td>
<td><strong>16K</strong></td>
<td><strong>1.4K</strong></td>
<td><strong>4</strong></td>
</tr>
</tbody>
</table>

* For ASIC gates ~= 10 x # of LUTs used. One RAM = 4Kb. One PLL also used.

### TX Device

<table>
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<td>-</td>
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<tr>
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</table>

### RX Device

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<tbody>
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<td><strong>1.4K</strong></td>
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This has been implemented in a pair of 2K LUT FPGAs.
Summary

• Trend towards modular systems
  – Notebooks, phones, drones, automotive, etc.

• Systems have a fair amount of low-speed signals
  – Control busses, GPIOs, LEDs, etc.
  – Routing congestions

• Signal aggregation/de-aggregation improves industrial design
  – Reduces connections

• Low power, small size FPGAs offer custom implementations

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