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MIPI-SPMISM 1.0 Multi-master Verification
Agenda

• MIPI-SPMI – An Introduction
• MIPI-SPMI Multi-master Verification Architecture
• Verification Challenges and their Solutions
• Conclusions and References
MIPI-SPMI – An Introduction

• SPMI (System Power Management Interface):
  – 2-wire serial interface
  – Supports up-to 4 masters and 16 slaves
  – Connects the integrated Power Controller (PC) of a System-on-Chip (SoC) processor system with one or more Power Management Integrated Circuits (PMIC) voltage regulation systems

• Within PC, SPMI-related functions are referred to as “Master”.
• Within PMIC, SPMI related functions are referred to as “Slave”.

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MIPI-SPMI – An Introduction

Figure 1 SPMI System Example
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MIPI-SPMI Multi-master Verification Architecture
Verification Challenges and their Solutions

- Multiple masters waking up at the same time and trying to connect
  - No RCS request
  - Pending RCS request
- Second master trying to connect when one master is already present
  - SSC Detection
  - Bus Idle
  - Bus Arbitration
- Multiple masters and slaves arbitrating with different priority levels
  - A-bit and SR-bit for slaves; priority and secondary MPLs for masters
Verification Challenges and their Solutions

- BOM (Bus Owner Master) transfer, i.e. SCLK Handover
- Disconnection of a master
  - Using TBO command
  - During command parity error
- Noise during
  - Bus Idle
  - Master Arbitration
  - Slave Arbitration
Multiple masters waking up at the same time and trying to connect

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Second master trying to connect when one master is already present
Multiple masters and slaves arbitrating with different priority levels and BOM (Bus Owner Master) transfer
Disconnection of a master

Figure 46 Transfer Bus Ownership Command Sequence
Noise on SDATA bus

Figure 26 False Bus Request Detection

Figure 28 False Slave Arbitration due to Noise

Figure 27 Noise During Priority Slots of the Bus Arbitration

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Conclusions and References

• MIPI-SPMI protocol plays a vital role in reducing the number of pin connections in a chipset as it supports multi-master and multi-slave systems and various types of data path commands.

• There are certain areas which need some improvement. Some of them have been addressed in MIPI-SPMI spec ver. 2.0. Some more are yet to be taken care as suggested by us in this presentation.

• **Reference:** MIPI® Alliance Specification for System Power Management Interface (SPMI) - Version 1.0 – 27 October 2008

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