Hezi Saar, Sr. Staff Product Marketing Manager
Synopsys

Driving 4K High-Resolution Embedded Displays in New Applications with MIPI DSI℠ and VESA DSC (Synopsys & Arm)
Agenda

• Rising demand for high resolution displays

• Arm® Mali®-Cetus Display processor

• Synopsys® DesignWare® MIPI DSI℠ Host Controller with VESA DSC Encoder

• Synopsys & Arm solution
Bandwidth Demand Increases for Embedded Displays

Meets the demands of vivid, detailed and immersive visual experience

- **Mobile:**
  - More powerful GPU, higher resolution cameras, richer content with high resolution and better visual quality drives the demand for mobile devices having a better displays.

- **VR/AR:**
  - Virtual reality application requires displays with not only high resolution but high refresh rate

- **Automotive:**
  - Dashboard/infotainment/mirrorless system displays with customized high resolutions and details demands bandwidth increases

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Arm Mali Display Overview

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Arm Mali Display in Arm Multimedia Subsystem

Feature Rich:
- Composition, scaling, rotation
- Gamma correction, colour management, co-processor interface, dual-display

Low power real-time performance:
- Single pass composition, Arm Frame Buffer Compression (AFBC), Optimized SMMU integration

Optimized software support:
- Android DDK
- Linux KMS
- Arm Mali Multimedia Suite

Supports all major display industry standards:
- MIPI, HDMI, VESA, CEA-861, ITU-R
Arm Mali Display processors - Driving Display Technologies

First architecture was designed for 1080p60, 1440p60, 1600p60 mobile/tablet displays

New architecture needed to address:

- Higher performance requirements (up to 4K120fps) driven by VR
- Quad scaling and more layers for Android N+ multi-window use case
- Power and quality optimizations for growing variety of panel and systems
- Composition for new disruptive UHD content (HDR10, HLG)

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Arm Mali-Cetus Architecture Overview

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Better Android Window Composition Capabilities

- Support for multi-window sessions in Android N
  - Optimized HWC Solver
- 8 composition layers when driving a single display
  - 4 layers per display output for dual display
- 4 scaled layers when driving a single display
  - 2 scaled layers per display output when driving a dual display
- Simultaneous layer + pixel alpha blending
  - Ideal for window animations
- Fully flexible and software programmable Z order
Flexible Use of Display Processor Resources

Software Layer Split and Layer Merge

- Software layer split and internal layer split of display layers with 2 scaling engines to optimize demanding downscaling use cases

Side by Side Processing

- Side-by-side processing for low voltage operation at 4Kp60-120fps
Performance, Area Comparison

Additional Functionality in Cetus

- 8 composition layers (vs 4 in DP650)
- Side-by-side processing
- Scaling split
- Uncompressed rotation removed from the real time path
- Higher AFBC decoder throughput
- Reduction of MMU latency

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Composition Scene: 2x4K (UHD) Graphics (32bpp) and 10-bit 4K (UHD) Video

Die Area

- DP650 + SMMU-500
- Cetus + SMMU-Tethra

TSMC 16FF+ LVT C16 7.5-track, 9-metal layers

Latency tolerance

Mali-DP650
Cetus
Cetus SBS
Display Output Unit

Backend Subsystem

Display Output Unit (DOU)

- Image Processing subsystem
- Backend subsystem

CU layer

Gamma, Dither, RGB2YCbCr

Line Split, YCbCr 4:2:0

Frame Timing, CMode

DOU 0

Side-by-Side Split

Link 0

Link 1

TETEXT / TETRIG

1:2 Display Split

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Synopsys & Arm Display Solution
Today’s Premium Smartphone

Smartphone Application – WQHD+

Step 1
WQHD 1440x2880 /60Hz/24bpp
1 stream at ~6.3 Gbps

Step 2
2:1 compression
1 stream at 3.16 Gbps

Step 3
DSI Port has 4 data lanes @ 1Gbps
Total bandwidth is 4Gbps

Mali- Cetus Display

Arm Application processor

WQHD+ is 270 Mhz pixel clock

VESA DSC v1.1 Encoder

MIPI DSI Host Controller v1.2

MIPI D-PHY℠ V1.2

MIPI DSI Host Controller + D-PHY

Ecosystem

WQHD

Display

Ecosystem

Display Driver #1

Master

4 data lanes
1 clock lane
AR/VR and Future Premium Smartphone

Smartphone VR Application – 4K+

**Step 1**
4320x2160 /90Hz/30bpp
1 stream at ~26.6 Gbps

**Step 2**
2 streams at ~13.3 Gbps

**Step 3**
3:1 compression
2 streams at ~4.44Gbps

**Step 4**
DSI Port has 4 data lanes @ 1.5Gbps

Mali-Cetus Display

Arm application processor

454 Mhz pixel clock

VESA DSC v1.1 Encoder

MIPI DSI Host Controller v1.2

MIPI D-PHY V1.2

Synopsys MIPI DSI +DSC Host Controller and D-PHY

Display Driver

Embedded Display Ecosystem

2160x4320p90
VESAT Display Stream Compression (DSC)

Enabling UHD Mobile Displays

- Visually lossless compression
  - Optimized for compression factor between 2x and 3x
- Intra-frame Constant Bit Rate (CBR) encoder
- Support 8, 10 and 12 bits per component
- RGB and YCbCr 4:4:4
- Based on Delta Pulse Code Modulation (DPCM) with an Indexed Color History (ICH)
- Requires a single line of pixel storage & rate buffer

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## DSC with Proven MIPI Specifications

<table>
<thead>
<tr>
<th>Resolution</th>
<th>Bandwidth</th>
<th>MIPI D-PHY v1.1 @ 1.5Gbps</th>
<th>MIPI D-PHY v1.2 @ 2.5Gbps</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>No compression</td>
<td>2x compression</td>
</tr>
<tr>
<td>FHD (1080x1920)</td>
<td>3.58 Gbps</td>
<td>3 lanes</td>
<td>2 lanes</td>
</tr>
<tr>
<td>WQHD (1440x2560)</td>
<td>6.37 Gbps</td>
<td>6 or 8 lanes</td>
<td>3 lanes</td>
</tr>
<tr>
<td>WQXGA (1600x2560)</td>
<td>7.08 Gbps</td>
<td>6 or 8 lanes</td>
<td>3 lanes</td>
</tr>
<tr>
<td>UHD (2160x3840)</td>
<td>14.33 Gbps</td>
<td>N/A</td>
<td>6 or 8 lanes</td>
</tr>
<tr>
<td>WQUXGA (2400x3840)</td>
<td>15.93 Gbps</td>
<td>N/A</td>
<td>6 or 8 lanes</td>
</tr>
<tr>
<td>5K (2880x5120)</td>
<td>25.49 Gbps</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>8K (4320x8192)</td>
<td>61.16 Gbps</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>

**Synopsys & Arm**
Synopsys MIPI DSI Host Controller with VESA DSC 1.1

- Fully integrated, cost-efficient solution to enable supporting ultra-high resolutions MIPI displays
- Complete DesignWare MIPI DSI Host Controller with VESA Display Stream Compression encoder and MIPI D-PHY easily integrates into application processors with less risk
- Integrated MIPI display IP reduces memory size and data transmission bandwidth to lower power consumption, area as well as EMI
- VESA DSC encoder allows higher refresh rates beyond 60Hz for drastically faster responsiveness and fluidity in ultra-high-resolution quad HD or 4K displays

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Integrating MIPI DSI + VESA DSC
Dual DSI Without DSC

Application Processor
- MIPI DSI Host Controller
- MIPI DSI Host Controller

Display Driver IC
- MIPI D-PHY
- MIPI D-PHY
- MIPI D-PHY
- MIPI D-PHY

Frame Buffer
- SDRAM
- SDRAM
- SDRAM
Remove DSI/D-PHY with Integrated DSI/DSC IP

Save Power, Area & Cost

- Remove
  - MIPI D-PHY Tx + DSI Ctrl
  - MIPI D-PHY Rx + DSI Ctrl
Remove SDRAMs with Integrated DSI/DSC IP

Save Power, Area & Cost

- Remove SDRAM
Save Power, Area and Cost with Scalable Architecture

- Less power
- Smaller system
- Lower cost
Enabling Challenging COG Connectivity

- Chip-on-Glass (COG) offers a thin profile, integrated display
  - At the same time has limitations in supporting high-switching frequencies
- VESA DSC Encoder IP reduces data transmission bandwidth
- Allows use of existing lower switching-speeds for higher-resolution displays
Reducing Number of Pins with D-PHY v1.2

- D-PHY v1.2 is getting adopted widely which enable 2.5Gbps/lane
- VESA DSC Encoder IP reduces data transmission bandwidth
- Allow drastic reduction in # of pins and power consumption
- D-PHY v1.2 capable design enables system flexibility

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Arm/Synopsys Provide Detailed Integration Guidelines

- Interface connectivity, clock and reset control
- Pixel data transfer in MIPI DSI Video Mode for both single and dual link
- Variable refresh rate in MIPI DSI Video Mode
- Synopsys eDPI interface and MIPI Command Mode operation
- Pixel data transfer in MIPI DSI Command Mode for both single and dual link
- Dynamic resolution change
- Partial update
- VESA Display Stream Compression (DSC) encoder integration
- Power control

Example: Arm Mali DPU and Synopsys DSI Host Controller utilizing DPI interface
Synopsys & Arm Display Solution

- Arm and Synopsys ensure complete and optimized end-to-end display solutions
- Arm and Synopsys reduce the complexities of porting & integration between apps processor and PHYs
- Joint application note available to our partners upon request providing configuration and integration guidelines