Dynamic Reconfiguration of UniPort-M Compliance Host
Background

• Day by Day we are slowly moving through the process of MIPI Globalization in Mobile Industry by converting all the available interfaces.

• In this process we have few Peripherals with common Interface i.e. MIPI UniPort-M = MIPI UniPro℠ + MIPI M-PHY®
Background
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• By using this common interface as a key element, am interested in developing the common host platform for validation of all the MIPI UniPort-M based peripherals.
Background
Known Limitation

• Based on this point, even though silicon vendors are ready with MIPI controllers (i.e. DUT’s) it’s taking huge time to develop Host Platforms for Validation of millions of DUT’s.
How to overcome this limitation?

• From this observation am coming up with a **Reconfigurable Host for all UniPort-M** based peripherals like Chip 2 Chip (i.e. IPC), WLAN, Storage (i.e. UFS). By using this platform we can switch between the host protocol’s on the fly, between IPC, WLAN and UFS.
System Level View

UFS+UniPro℠ — MEMORY

C2C+UniPro℠ — C2C

HOST M-PHY® — DUT M-PHY®

WLAN+UniPro℠ — WLAN Modem
Benefits of this Platform

• The major advantage of designing this kind of host platform was to reduce the HW development time for Protocol specific Host and cost as well.

• We can easily upgrade’s the Host Protocol according to the latest changes in MIPI Specification.

• Easy to debug FPGA when compared with ASIC.
Benefits of this Platform

• Can validate all the Power Saving Technique’s described in MIPI specification.
• We can control and mount different Power Modules on this platform so as to support different voltage requirement’s as per specification.
Reconfigurable Host Platform

- Micro-Processor
- FPGA
- RMMI TX
- RMMI RX
- CONTROL
Reconfigurable Host implementation details

• All the protocol specific combinations will be pre-loaded in Flash.
• Host can re-configure from one protocol to other just by switching between the preloaded images.(i.e. RTOS/OS + FW + Bitfile)
Advantages of this Solution

- Single HW resource can be used to Validate multiple protocols.
- Different BSP can be developed, specific to the different OS or RTOS according to the requirement from Architecture.
- Parallel FW Teams can work on different peripheral interfaces.
Internals of System

Applications
Operating System
Hardware Interface

Processor Sub System

Processor
RAM

FPGA

Peripheral A
Peripheral B
Peripheral C

AXI
Internals of System

• The SW-HW interface can be varied from Protocol to Protocol requirement like AXI, APB, AHB...etc
• As of now we can handle all these kinds of BUS interface by using bridges.
Complete System Level View
Complete System Level View

• By using Reconfiguration Technique we can reduce the HW cost and do the Effective utilization of HW resources.
• We can maintain the Host Platform Form Factor so that chambers can also be common for different protocols.
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