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MIPI CSI-2℠ for Multi-camera, Long Range Use Cases and Implementation Methods Using FPGAs

2017 MIPI ALLIANCE DEVELOPERS CONFERENCE

BANGALORE, INDIA
MIIPI.ORG/DEVCON
Agenda

- MIPI CSI-2 Introduction & Features
- Camera Market & Projections
- Multi-camera & Long Distance Use Case(s)
- System Requirements
- Value of FPGA for MIPI CSI-2
- Q & A
mipi.org

- MIPI Alliance: Developing the world’s most comprehensive set of interface specifications for mobile and mobile-influenced products.
MIPI CSI-2 Features

Note: MIPI CSI-2^{SM} 1.1, MIPI D-PHY^{SM} 1.1 considered in this presentation.

- Multi-lane support (1.5Gbps/Lane)
- Multiple data types (RAW, RGB, YUV)
- Interleaving (VC, Data type)
MIPI CSI-2 Features

DATA IDENTIFIER (DI):
Contains the Virtual Channel Identifier and the Data Type Information
Data Type denotes the format/content of the Application Specific Payload Data.
Used by the application specific layer.

16-bit WORD COUNT (WC):
The receiver reads the next WC data words independent of their values.
The receiver is NOT looking for any embedded sync sequences within the payload data. The receiver uses the WC value to determine the end of the Packet.

8-bit Error Correction Code (ECC) for the Packet Header:
8-bit ECC code for the Packet Header. Allows 1-bit errors with the packet header to be corrected and 2-bit errors to be detected.

APPLICATION SPECIFIC PAYLOAD CHECKSUM (CS)

32-bit SHORT PACKET (SH)
Data Type (DT) = 0x00 – 0x0F

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MIPI CSI-2 Features

Data Identifier (DI) Byte

Virtual Channel Identifier (VC)  Data Type (DT)

Channel Identifier

Channel Configuration

Data In

Channel Detect

Logical Channel Control

Channel 0  Channel 1  Channel 2  Channel 3

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Camera Projections

- Camera market by application

North America camera module market by application, 2012 - 2022, (USD Million)

Source: grandviewresearch.com

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Automotive-ADAS Projections

ADAS Sensor growth (1000s)

Source: IHS

ADAS Semiconductor forecast (1000s), Image Sensors not included

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Video Surveillance Projections

Source: IHS

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Multi-camera Systems

How many cam’s can be supported?
System level aspects in such designs

- Bandwidth
- Protocol support
- Mux Chip support

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- Bandwidth
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- IO Support

Type-1

Type-2
System aspects-Type1

How many cam’s can be supported? System level aspects in such designs

- Total bandwidth available
- Interleaving as supported MIPI CSI-2 Specification
- Maximum input channels supported by mux chip
System aspects-Type2

- Protocol support
- Mux Chip support
- IO Support

How many cam’s can be supported?

System level aspects in such designs

- Total bandwidth available
- Interleaving as supported MIPI CSI-2 Specification
- Maximum input channels supported by mux chip
- Maximum CSI-2 Instances that can be implemented on the chip

VC=0, RAW8
VC=1, RAW8
VC=2, RAW8
VC=3, RAW8

VC=0, RAW10
VC=1, RAW10
VC=2, RAW10
VC=3, RAW10

VC=0, RAW12
VC=1, RAW12
VC=2, RAW12
VC=3, RAW12

VC=0, RAW8
VC=1, RAW8
VC=2, RAW8
VC=3, RAW8

VC=0, RAW10
VC=1, RAW10
VC=2, RAW10
VC=3, RAW10

VC=0, RAW12
VC=1, RAW12
VC=2, RAW12
VC=3, RAW12
System Requirements-Type1

- 1920x1080 @ 30fps, RAW8 -> Requires ~0.74Gbps

Bandwidth

1.5Gbps, 4L=6

4/0.74=8

Interleaving

VC=4

4*1=4

Mux Chip

Based on Chip

min(8,4,4)=4

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System Requirements-Type2

- 1920x1080 @ 30fps, RAW8 -> Requires ~0.74Gbps

**Bandwidth**
- 1.5Gbps, 4L=6
- \( \frac{6}{0.74} = 8 \)

**Interleaving**
- VC=4
- DT=1(RAW8)
- \( 4 \times 1 = 4 \)

**Mux Chip**
- Based on Chip
- Lets say ‘4’

**IO Support**
- Based on FPGA IO
- \( \min(8,4,4) = 4 \)
- CSI-2 Instances = 8
- Max Cam’s = 4*8 = 32

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AutoGrade US+ supports 8 Instances with Native IO’s
Multi-camera & Long Distance Use Case(s)

Source: mipi.org

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Long Distance Using Bridge IC’s

**MIPI Interfaces may be converted to/from these high speed transports in bridge chips when length exceed MIPI Specification lengths**

- **Mux Chip**
- **Bridge IC**
- **Video Processing**
- **Bridge IC**

Supported cable length, data rate determined by Bridge IC

Converting MIPI D-PHY$^{\text{SM}}$ to LVDS

Converting LVDS to MIPI D-PHY$^{\text{SM}}$

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Value of FPGA for MIPI CSI-2

- Most flexible & scalable platform for maximum reuse and best TTM
  - Implement End-to-End systems with ease
- Latest FPGAs can speak MIPI D-PHY
  - Single Chip(PHY+Controller), reduces BOM. More D-PHY interfaces per chip ( > 16)
  - Flexible interfaces: Lanes (1,2,3,4), Data rates, VC filtering etc..
- Latest FPGAs built on a common real-time processor and programmable logic equipped platform enables unlimited possibilities for next generation ADAS applications
  - Innovative ARM® + FPGA architecture for differentiation, analytics & control
Q & A

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