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MIPI I3C℠ Interface – Advanced Features
Outline

• MIPI I3C℠ – intelligent multifeatured interface
• List of main bus management procedures
• Timing Control
  – Problems solved, Challenges, Practical implementation aspects
• Elements of flow control
  – Problems solved, Challenges, Practical implementation aspects
MIPI I3C℠ – Intelligent Multifeatured Interface

- MIPI I3C℠ supports several communication formats, all sharing a two-wire interface.
  - The two wires are designated SDA and SCL:
    - SDA (Serial Data) is a bidirectional data pin
    - SCL (Serial Clock) can be either a clock pin or a data pin while in certain HDR Modes

- An MIPI I3C℠ Bus supports the mixing of various Message types:
  - I²C-like SDR Messages, with SCL clock speeds up to 12.5MHz
  - Broadcast and Direct Common Command Code (CCC) Messages that allow the Master to communicate to all or one of the Slaves on the I3C Bus, respectively
  - HDR Mode Messages, which achieve higher data rates per equivalent clock cycle
  - I²C Messages to Legacy I²C Slaves
  - Slave-initiated requests to the Master, for example for In-Band Interrupt or to request the Master role
MIPI I3C℠ BUS Management Features

- Dynamic Address Assignment
- Hot-Join
- In-Band Interrupt
- Secondary Master
- In-Band Hard RESET
- Timing Control
- Common Command Codes
- Error detection and Recovery
- Elements of Flow Control
Timing Control

• Complex applications require several Sensors on a common timeline
• Synchronous Systems and Events
  – Controlling the sampling moments has the potential of drastically reducing the system energy expenditure
• Asynchronous Systems and Events
  – The accuracy of the timestamps of events matters
• The Synchronous and Asynchronous modes can be used independently and concurrently on the same bus and devices
Synchronous Systems and Events

SYNC Tick [ST] and Delay Time [DT] in-band, via I3C bus

Sequence Repetition Period
Adjustable [0.2 ; 5 sec], 1 sec nominal
Synchronous – Multiple Transactions

- **I3C START**
  - ST&DT Polling
  - Polling or something else
  - ST&DT Polling

- **Sensors Sample unsynchronized**
  - Sync Tick [ST] & Delay Time [DT]
  - ST if validated by DT
  - T_Ph start, calculated from ST and DT
  - Refresh/Adjust Sensor’s Timer
  - DT between ST and T_Ph Start
  - Sequence Repetition Period
    - Adjustable [0.2 : 5 sec], 1 sec nominal

- **I3C messages, on the bus**
  - Some I3C transactions START condition is used by the Slaves (sensors) for adjusting their (sensors’) internal timers
  - Sensors Sample unsynchronized
  - Sensors Sample in sync
  - ST&DT to next ST&DT delay
    - Adjustable [0.2 ; 5 sec], 1 sec nominal
    - Each ST&DT instantiation includes Timer Error Correction data

- **Sequence repeats**
  - Sensors Sample in sync
  - T_Ph start, calculated from ST and DT
  - ST&DT Polling
Synchronous – Common Command Codes

• SETXTIME CCC

• Configuration messages
  – ODR (Output Data Rate)
  – TPH (Procedure Repetition Time)
  – TU (Time Unit)

• Run Time messages
  – SYNC Tick [ST]
  – Delay Time [DT]
Asynchronous Systems and Events

• Four Async Modes
  – Basic – Async Mode 0
  – Enhanced – Async Mode 1, 2 and 3

• SETXTIME is the CCC
  – The defining byte selects the running mode
Async 0 Time Diagram

MTS – Master Timestamp, expressed in MASTER’s time units

MREF – Master Reference, i.e. Start of Master’s secondary counter, MCNT2

MC1, MC2 – Master’s counters values, captured at the corresponding HWSE events.

SC1, SC2 – Slave’s counters values, captured at the corresponding HWSE events.

MTS = MREF – MC2×SC1/SC2
Async 0 on SDR
Elements of Flow Control

• The Transmitter drives actively the data lines
  – SDA on HDR-DDR
  – SDA and SCL on HDR-TSx

• The Receiver might need to end the transaction
  – The bus needs to provide the opportunity for the Receiver to change the state of a line, in a pre-established way
# HDR-DDR Transactions

## HDR-DDR Preamble Values

<table>
<thead>
<tr>
<th>Context</th>
<th>Preamble Value and Interpretation</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2’b00</td>
</tr>
<tr>
<td>After EnterHDR</td>
<td>Command Word follows</td>
</tr>
<tr>
<td>After Read CMD</td>
<td>-</td>
</tr>
<tr>
<td>After Read DATA</td>
<td>CRC Word follows</td>
</tr>
<tr>
<td>After Write CMD</td>
<td>-</td>
</tr>
<tr>
<td>After Write DATA</td>
<td>CRC Word follows</td>
</tr>
</tbody>
</table>
HDR-DDR – Slave controls DDR READ command
HDR-DDR – Master Controls DDR READ Transaction [1]
HDR-DDR – Master Controls DDR READ Transaction [2]
HDR-DDR – Slave Requests DDR WRITE Termination [1]

Early ending with no CRC
HDR-DDR – Slave Requests DDR WRITE Termination [2]
HDR-TSx – Master Controls S2M Data Transfer
HDR-TSx – Slave Controls the M2S Data Transfer
ENDXFER CCC – Early Termination Setup and Invocation

- Defining Bytes
  - 0x7F – SET/GET Repetition Interval for HDR-TSx
  - 0x55 – Initiates the HDR-TSx with Ending Data Transfer Procedure Enabled
  - 0xF7 – SET/GET CRC Index for HDR-DDR
  - 0xAA – Initiates the HDR-DDR with Ending Data Transfer Procedure Enabled

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**Defining**

<table>
<thead>
<tr>
<th>S</th>
<th>7’h7E / W / ACK</th>
<th>ENDXFER CCC / T</th>
<th>Defining Byte / T</th>
<th>(Optional) Data / T</th>
<th>Sr</th>
<th>P</th>
</tr>
</thead>
</table>

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**Diagram**

- Describes Slave
  - Repeat for additional Slaves on ENDXFER

- ENDXFER has ended
  - Next CCC
  - 7’h7E / W / ACK
  - Slave Addr / RnW / ACK
  - P
  - P
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