Hezi Saar, Sr. Staff Product Marketing Manager
Synopsys

Enabling Higher Data Rates and Variety of Channels with MIPI D-PHY℠
Agenda

- Design motivation
- MIPI D-PHY evolution
- Summary of MIPI D-PHY specification
- MIPI channel evolution
- Channel modeling results in ADS
- Specification run through for D-PHY v2.1
- MIPI D-PHY 3.0 approved roadmap
Design Motivation

• Higher data rate
• Adaption to newer technologies
• Longer channel length, channel evolution
• Backward compatible
• Reliable with sufficient margins
• Augmenting existing eco system
• Meeting camera and display present and future needs
• Growing market applications and segments
• The de-facto standard for camera and display
• Target automotive segment for ADAS applications

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MIPI D-PHY Evolution

• D-PHY 1.0  1.0 Gbps
• D-PHY 1.1  1.5 Gbps
• D-PHY 1.2  2.5 Gbps
• D-PHY 2.0/2.1 4.5 Gbps
• D-PHY 3.0  10-14 Gbps

Higher data rate enables high pixel count cameras and displays
Basic PHY Architecture

Ref Clock Controls

APPI = Abstracted PHY-Protocol Interface (complete PHY, all lanes)
PPI = PHY Protocol Interface (per lane, some signals can be shared with multiple lanes)
Lane Module
<table>
<thead>
<tr>
<th>Spec Parameters</th>
<th>D-PHY 3.0</th>
<th>D-PHY 2.0/2.1</th>
<th>D-PHY 1.2</th>
<th>D-PHY 1.1</th>
<th>D-PHY 1.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Rate</td>
<td>10-14 Gbps</td>
<td>4.5Gbps</td>
<td>2.5Gbps</td>
<td>1.5Gbps</td>
<td>1Gbps</td>
</tr>
<tr>
<td>HS Tx Differential Voltage</td>
<td>140-270mV</td>
<td>140-270mV</td>
<td>140-270mV</td>
<td>140-270mV</td>
<td>140-270mV</td>
</tr>
<tr>
<td>HS Tx Single Ended Output Impedance</td>
<td>40-62.5ohms</td>
<td>40-62.5ohms</td>
<td>40-62.5ohms</td>
<td>40-62.5ohms</td>
<td>40-62.5ohms</td>
</tr>
<tr>
<td>HS Tx Common Mode Static Voltage</td>
<td>150-250mV</td>
<td>150-250mV</td>
<td>150-250mV</td>
<td>150-250mV</td>
<td>150-250mV</td>
</tr>
<tr>
<td>HS Tx Rise/Fall Times (20-80%)</td>
<td>TBD</td>
<td>30-100ps(4.5Gbps)</td>
<td>50ps-0.4UI</td>
<td>100ps-0.35UI</td>
<td>100ps-0.3UI</td>
</tr>
<tr>
<td>Tx Cpad Target (Driven by return loss in the spec)</td>
<td>TBD</td>
<td>3pF</td>
<td>3.3pF</td>
<td>3pF</td>
<td>3pF</td>
</tr>
<tr>
<td>HS Tx De-emphasis</td>
<td>TBD</td>
<td>-3.5dB(+/-1dB) -6dB(+/-1dB)</td>
<td>None</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>Spread Spectrum Clocking</td>
<td>ModulationRate<del>30-33KhZ SSC Deviation</del>5000PPM Down Spread</td>
<td>ModulationRate<del>30-33KhZ SSC Deviation</del>5000PPM Down Spread</td>
<td>None</td>
<td>None</td>
<td>None</td>
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<tr>
<td>Scrambling</td>
<td>Yes Need to be supported by the Controller</td>
<td>Yes Need to be supported by the Controller</td>
<td>None</td>
<td>None</td>
<td>None</td>
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<tr>
<td>Spec Parameters</td>
<td>D-PHY 3.0 (In progress)</td>
<td>D-PHY 2.0</td>
<td>D-PHY 1.2</td>
<td>D-PHY 1.1</td>
<td>D-PHY 1.0</td>
</tr>
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<td>-----------</td>
</tr>
<tr>
<td>HS Tx Timing</td>
<td>TBD</td>
<td>TJ<del>0.3UI DJ</del>0.2UI RJ<del>0.1UI All Jitter relative to clock Static Skew Clock to Data</del>0.0 to 0.2UI</td>
<td>TJ<del>0.3UI All Jitter relative to clock Static Skew Clock to Data</del>0.0 to 0.2UI</td>
<td>Data to Clock Skew~0.2 to 0.2UI</td>
<td>Data to Clock Skew~0.15 to 0.15UI</td>
</tr>
<tr>
<td>HS Tx AC CM Noise</td>
<td>15mVrms(&gt;450Mhz) 25mVpk-pk(50-450Mhz)</td>
<td>15mVrms(&gt;450Mhz) 25mVpk-pk(50-450Mhz)</td>
<td>Same as DPHY2.0</td>
<td>Same</td>
<td>Same</td>
</tr>
<tr>
<td>BER</td>
<td>1e-12</td>
<td>1e-12</td>
<td>1e-12</td>
<td>1e-12</td>
<td>1e-12</td>
</tr>
<tr>
<td>LP Tx Output High Level</td>
<td>TBD</td>
<td>0.95-1.05</td>
<td>0.95 to 1.3V</td>
<td>1.1-1.3</td>
<td>1.1-1.3V</td>
</tr>
<tr>
<td>LP Tx Min Slew Rate</td>
<td>TBD</td>
<td>25mV/ns</td>
<td>25mV/ns</td>
<td>30mV/ns</td>
<td>30mV/ns</td>
</tr>
<tr>
<td>LP Tx Max Slew Rate</td>
<td>TBD</td>
<td>500mV/ns(0pF Load) 300mV/ns(5pF Load) 250mV/ns(20pF Load) 150mV/ns(70pF Load)</td>
<td>Same as DPHY2.0</td>
<td>Same</td>
<td>Same</td>
</tr>
<tr>
<td>Channel Loss</td>
<td>MPHY Spec Channel2 (7-14inch)</td>
<td>MPHY Spec Channel2 (7-14inch)</td>
<td>MPHY Spec Channel2 (7-14inch)</td>
<td>DPHY Spec Channel (5-11inch)</td>
<td>DPHY Spec Channel (5-11inch)</td>
</tr>
<tr>
<td>Channel ISI</td>
<td>TBD</td>
<td>0.2UI</td>
<td>0.2UI</td>
<td>+/-0.1UI</td>
<td>+/-0.2UI</td>
</tr>
<tr>
<td>Channel Clk to Data Statix Skew</td>
<td>TBD</td>
<td>+/-0.1UI</td>
<td>+/-0.1UI</td>
<td>None(Included in Channel ISI)</td>
<td>None(Included in Channel ISI)</td>
</tr>
<tr>
<td>Spec Parameters</td>
<td>D- PHY 3.0</td>
<td>D- PHY 2.0</td>
<td>D- PHY 1.2</td>
<td>D- PHY 1.1</td>
<td>D- PHY 1.0</td>
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<td>---------------------------------------------------------------------------</td>
<td>---------------------------------------------------------------------------</td>
<td>---------------------------------------------------------------------------</td>
<td>---------------------------------------------------------------------------</td>
<td>---------------------------------------------------------------------------</td>
</tr>
<tr>
<td>HS Rx Deskew</td>
<td>Internal Clock to Data using Tx Calibration Pattern</td>
<td>Internal Clock to Data using Tx Calibration Pattern</td>
<td>Internal Clock to Data using Tx Calibration Pattern</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>HS Rx Differential Input Threshold</td>
<td>TBD</td>
<td>+40mV to -40mV</td>
<td>+40mV to -40mV</td>
<td>+70mV to -70mV</td>
<td>+70mV to -70mV</td>
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<tr>
<td>HS Rx Common Mode DC</td>
<td>TBD</td>
<td>70-330mV</td>
<td>70-330mV</td>
<td>70-330mV</td>
<td>70-330mV</td>
</tr>
<tr>
<td>HS Rx Differential Input Impedance</td>
<td>80-125ohms</td>
<td>80-125ohms</td>
<td>80-125ohms</td>
<td>80-125ohms</td>
<td>80-125ohms</td>
</tr>
<tr>
<td>HS Rx Common Mode Noise Tolerance</td>
<td>TBD</td>
<td>100mV(pk-pk)</td>
<td>100mV(pk-pk)</td>
<td>200mV(pk-pk)</td>
<td>200mV(pk-pk)</td>
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<tr>
<td>HS Rx Jitter Tolerance</td>
<td>TBD</td>
<td>Tjtol~0.5UI</td>
<td>Tjtol~0.5UI</td>
<td>No Independent Jitter Spec</td>
<td>No Independent Jitter Spec</td>
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<tr>
<td>HS Rx Skew Tolerance</td>
<td>TBC</td>
<td>Static Skew of +/-0.3UI between Clock and data</td>
<td>Static Skew of +/-0.3UI between Clock and data</td>
<td>Setup/Hold~0.2UI</td>
<td>Setup/Hold~0.15UI</td>
</tr>
<tr>
<td>HS Rx Common Mode Voltage DC</td>
<td>TBD</td>
<td>70-330mV</td>
<td>70-330mV</td>
<td>70-330mV</td>
<td>70-330mV</td>
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<tr>
<td>HS Rx Common Mode Termination</td>
<td>TBD</td>
<td>14pF-60pF</td>
<td>14pF-60pF</td>
<td>2-60pF</td>
<td>2-60pF</td>
</tr>
<tr>
<td>Spec Parameters</td>
<td>D-PHY 3.0</td>
<td>D-PHY 2.0</td>
<td>D-PHY 1.2</td>
<td>D- PHY 1.1</td>
<td>D- PHY 1.0</td>
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</tr>
<tr>
<td>LP Rx Min Input Voltage</td>
<td>TBD</td>
<td>740mV</td>
<td>740mV</td>
<td>880mV</td>
<td>880mV</td>
</tr>
<tr>
<td>LP Rx Min Pulse Width</td>
<td>TBD</td>
<td>20ns</td>
<td>20ns</td>
<td>20ns</td>
<td>20ns</td>
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<tr>
<td>PPI Data Bus Width</td>
<td>TBD</td>
<td>8/16/32 bit</td>
<td>8bit</td>
<td>8bit</td>
<td>8bit</td>
</tr>
<tr>
<td>COG Channel Support for Displays</td>
<td>Yes WIP Plan to support higher channel loss for displays</td>
<td>Yes WIP Plan to support higher channel loss for displays</td>
<td>None</td>
<td>Not Known</td>
<td>-</td>
</tr>
</tbody>
</table>

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Differential Insertion Loss Comparison

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**Tx+ Short Channel+ Termination (Tx Eye Diagram)**

- **Transmit Swing**: +140 to -140 mV
- **Tx Impedance**: ~62.5 ohms
- **Tx Deemp**: None
- **EqMode**: Specify de-emphasis
- **Tx Lip (Rx) Diff**: +140 to -140 mV
- **Rx Eye Diagram**: Hex Eye Width ~ 0.16UI
  - Eye Width ~ 0.54 UI

**Synopsys**
Tx+ SpecChannel + Termination

Eye Height ~86mV
Eye Width ~ 0.577UI

Transmit Swing~+140 to -140mV
Tx Impedance~62.5ohms
Tx Deemp~None
Tx Cpin~3pF

Eye Height ~88mV
Eye Width ~ 0.576UI

Synopsys
Tx+ SpecChannel + Termination (9Gbps)

- Data Rate = 9 Gbps
- Pattern PRBS9
- Tx de-emphasis = 7dB
- Tx output impedance 125 ohm
- Cpad = 1.5 pf
- Channel Reference 2
- Rx termination 80 ohm
- Rx equalization CTLE adaptable.
- Zero1 = 840 Mhz
- Pole 1 = 1.048 Ghz
- Pole 2 = 9.586 Ghz
- DC_gain 1.98776
- Rx DFE Adaptive 2 tap

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Overall Leoni Channel Performance

\[ \text{Eqn dphy12}_{x} = [1.25e9, 1.25e9, 2.5e9, 3.75e9, 3.75e9, 2.5e9, 1.25e9] \]
\[ \text{Eqn dphy12}_{y} = [-3.25, -4.25, -6.9, -9.6, -8.6, -5.9, -3.25] \]
\[ \text{Eqn dphy2}_{\text{final short}} = [-1.1, -1.9, -5.4, -4.3, -1.1] \]
\[ \text{Eqn dphy2}_{\text{final standard}} = [-3.25, -4.25, -12.5, -11.1, -3.25] \]
\[ \text{Eqn dphy2}_{\text{final long}} = [-5.7, -6.7, -20.8, -19.2, -5.7] \]
\[ \text{Eqn dphy2}_{\text{final x}} = [1.25e9, 1.25e9, 5.0e9, 5.0e9, 1.25e9] \]
Rosenberger RG174

![RG174 Channel Graph](image_url)
Rosenberger RG5811

RG5811 Channels

- Rosenberger 5 meter
- MIPI Short Channel
- Rosenberger 10 meter
- Rosenberger 15 meter
- MIPI Reference Channel
- MIPI Long Channel

freq. GHz
Fakra Connector Modeling

- TDR performance:
  - ADS generated equivalent models
  - S-parameter model/TDR profile

Source: Keysight Technologies

Synopsys
Modes of operation
Summary

• MIPI D-PHY
  – Is the de-facto standard for camera and display connectivity
  – Operates at 4.5 Gbps over multiple lanes
  – Enables SoCs for emerging applications: automotive infotainment and advanced driver assistance systems (ADAS), allowing higher data transmission over longer channels
  – Provides flexibility, speed, power and cost benefits
  – Uses low-latency transitions between high-speed and low-power modes with high noise immunity and high jitter tolerance

Synopsys
MIPI D-PHY 3.0

- Data rate 10 to 14 Gbps
- Support for automotive grade PHY requirements with long channels
- Transitions to embedded clock above a defined data rates
- Remains backward compatible to MIPI D-PHY 2.1
Synopsys® DesignWare® MIPI IP Portfolio