TECHNOLOGY BRIEF

Low Latency Interface (LLI) v2.1

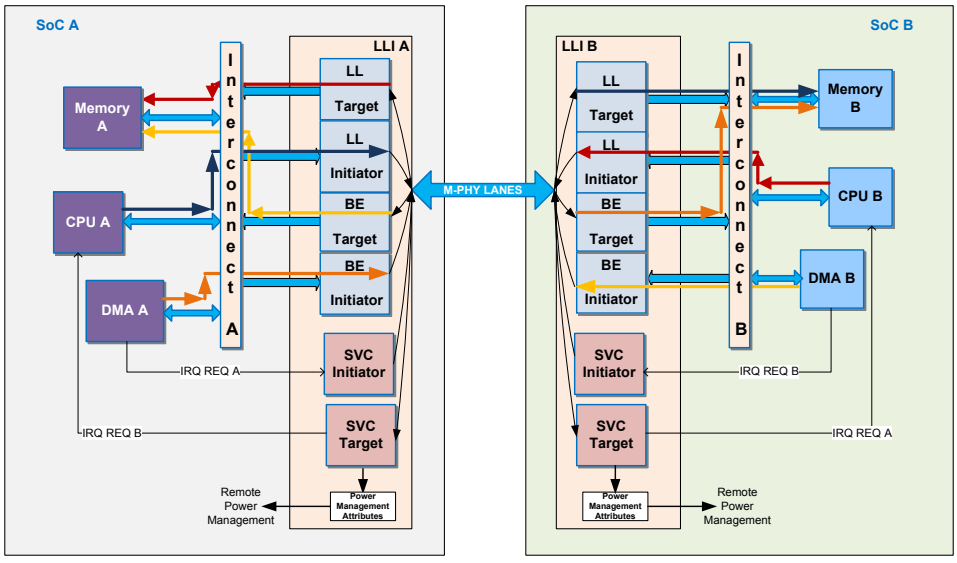
Specification Overview

MIPI Low Latency Interface v2.1 is a point-to-point interconnect that allows two devices on separate chips to communicate as if a device attached to the remote chip is resident on the local chip. Devices on this bidirectional connection use memory mapped transactions for communications via native protocols such as Open Core Protocol and Advanced Microcontroller Bus Architecture (AMBA®), using the MIPI M-PHY® physical layer.

As its primary use case, LLI targets concurrent low latency and high bandwidth chip-to-chip traffic over a low pin count interface, using any of three functionally oriented traffic classes: Service, Best Effort and Low Latency. Each provides an efficient mechanism for optimal data routing between the variety of devices supported by LLI, from direct HW-to-HW signaling and interrupts (using Service Traffic Class) to the high bandwidth, high volume data streams (bulk DMA transfers using Best Effort Traffic Class) to the occasional low bandwidth latency-critical transfers (cache refill traffic using Low Latency Traffic Class). Semantics of the Service Transaction signals are not specified and can be used for any purpose to reduce pin count on both sides of the link.

LLI offers simultaneous support for multiple parallel communication flows in both directions for all three traffic classes without significant degradation in latency for low latency traffic and in bandwidth for best effort traffic and with independent transactions initiation from either side of the link.

The LLI Specification describes a layered, transaction-level protocol, where Targets and Initiators on two linked chips exchange Transactions without software intervention. Software is used to initialize the LLI Stack at boot time, to manage errors handling, and to re-configure the LLI Link. . This approach reduces latency and allows software compatibility regardless of the partitioning of the hardware on the two linked chips.



Example of LLI Environment

SPECIFICATION BRIEF

Low Latency Interface (LLI) v2.1

FEATURES

Target Applications

- Low latency, reduced pin count inter-chip communication in mobile and battery operated devices: Application processors, Modems, Hardware Accelerators, Co-processors and Companion Chips

Key Features

- Combines key advantages of serial (low pin count, ease of routing) and parallel (low latency/high bandwidth) interfaces
- Low latency, low power serial interface supporting real-time multi-chip architectures
- Seamless transition from multi-chip to integrated single chip implementations
- Supports tightly coupled IPC communication based on memory sharing, utilizing direct memory access

High Link Efficiency

- A new 36 symbol transmission format (PHIT-36) and new Frame format (Extended Data Frame) improve link efficiency from 53.33% to 71.11% (including 8b10b encoding).

Power Management Support

- LLI v2.0 defines four new attributes to enable better system power management:
  - Wakeup latency bound
  - Resource Power OFF
  - Resource Power ON
  - Resource Power ACK

Inter Processor Communication (IPC) Support

- LLI v2.1 defines a new class of attributes for easier support of IPC between two chips, intended for use by IPC protocol

BENEFITS

- Efficient System Partitioning
- Very low latency (using 12 symbol transmissions)
- Supports 3 traffic classes for simultaneous low latency and high bandwidth communication:
  - Service (SVC)
  - Low Latency (LL)
  - Best Effort (BE)
- Minimal or no software housekeeping
- In-band signaling minimizes extra inter-chip General Purpose Input Outputs (GPIOs) and pin count
- Asymmetric M-PHY lanes implementation support reducing M-PHY link pins count
- HS- Gear 3 Support for MIPI M-PHY Physical Layer

Scrambling to reduce EMI

- LLI v2.1 defines two optional features, a scrambling function to be applied on the data that is transmitted, and a new type of filler transmission to mitigate electromagnetic interference (EMI) that would otherwise be introduced by repetitive transmission of same M-PHY Symbol(s).

Increased link speed and M-PHY capability attribute updates

- LLI v2.1 supports HS-Gear 2 of the MIPI M-PHY Specification in addition to HS Gear1 already supported in LLI, enabling raw transmission rates of up to 2.9 Gigabit/sec.