MIPI® Physical Layer and Protocol Testing Solutions
Agenda

- MIPI® Standards Overview
- Tek Strategic Involvement in MIPI
- D-Phy testing
  - Tx, & CSI-DSI Decode
  - Rx
- M-Phy testing
  - Tx, & Decode
  - Rx
- DSI &CSI testing - Stimulus
- DSI &CSI testing - Protocol Validation
- SLIMbus &H.S.I testing
- DigRF testing
- Summary, Q&A
MIPI Standards Overview
Example of Mobile Device

MIPI Physical-layer standards are:
D-PHY, M-PHY, SlimBus, DigRF 3G

MIPI Protocol-layer standards are:
CSI, DSI, DigRF 3G, DigRF 4G
MIPI Standards Overview
Example Mobile Device Block Diagram

**MIPI Specific Standards**

- **Display Unit**
  - DSI
  - Display Driver IC
  - DSI

- **CMOS Image Sensor**
  - CSI
  - Camera Driver IC
  - CSI

- **Audio Driver IC**
  - SLIMbus

- **Loudspeaker**
- **Ear Piece**
- **FM Radio**
- **Microphone**

**Baseband IC**
- Apps Processor
- HSI
- Tx/Rx Processor

**RF IC**
- DigRF
- RF Interface (WCDMA, GSM, WLAN, FM, Bluetooth, GPS, MobileTV, etc)

**Memory Interfaces**
- Memory (Internal)
- Memory (SD Card)
  - (ex. Mobile DDR, Mobile SDRAM, Flash, etc)

**Air Interfaces**
- (ex. WiMax)

**Definitions**
- CSI = Camera Serial Interface
- DSI = Display Serial Interface
- SLIMbus = Serial Low-power Inter-chip Media Bus

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Oscilloscope Fundamentals - © 2011 Tektronix
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Tek Strategic Involvement with MIPI Alliance & UNH-IOL

- Tektronix is a **Contributor Member** of the MIPI Alliance
- Tektronix is actively-participating in several MIPI Working Groups
- Tektronix has a close working relationship with UNH-IOL.

**Combined Tek Press-Release with UNH & MIPI Alliance in Sept-2010:**

- [http://www2.tek.com/cmswpt/prdetails.lotr%3Fct%3DPR%26cs%3DNews%2BRelease%26ci%3D17639%26lc%3DEN&urlhash=HZu6](http://www2.tek.com/cmswpt/prdetails.lotr%3Fct%3DPR%26cs%3DNews%2BRelease%26ci%3D17639%26lc%3DEN&urlhash=HZu6)

- “…….Tektronix is spurring the adoption of D-PHY and M-PHY specifications. Tektronix is aiding the adoption of the new M-PHY interface by giving designers the testing tools they need to ensure signal integrity and verify performance of increasingly complex designs.”
  - **Joel Huloux, Chairman of the MIPI Alliance.**

- “Tektronix has been supportive of UNH-IOL's collaborative efforts……,”
  - **Andy Baldman, Senior technical staff, R&D, UNH-IOL.**
Tek Tools are listed on MIPI Alliance Webpage and CTS

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Tek MIPI setup used by UNH-IOL

Through a collaborative agreement with Tektronix, the UNH-IOL is using the Tektronix DSA72004B Digital Serial Analyzer for MIPI testing. Combined with UNH-IOL’s D-PHYGUI software, this platform provides the ability to capture and analyze D-PHY signalling, in order to perform the UNH-IOL D-PHY Transmitter Physical Layer Conformance Test Suite.

For more information on the Tektronix DSA72004B please visit http://www.tek.com

The Moving Pixel Company P331 MIPI D-PHY Probe is used to implement many protocol layer tests for both CSI-2 and DSI for up to 4 lanes.


UNH-IOL (University of New Hampshire) is a 3rd party test house for MIPI testing
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What is D-PHY?

- It’s a PHY standard for interfacing Camera (CSI) & Display (DSI)
- Two modes of transmission
  - High Speed (HS) and Low Power (LP)
- Modes are mixed during the operation
  - Transitions from LP to HS and back to LP on the fly
- Maximum Data Rate
  - High Speed mode: 80 Mbps – 1.5 Gbps, Typically at ~500 Mbps.
  - Low Power mode: Up to 10 Mbps
- Bus termination
  - 50 ohms in HS
  - Hi-Z in LP
D-PHY Testing Challenges

- Logo testing is not required, but Optional.
  - MIPI is Chip-to-Chip/ Chip-to-Peripheral interface, similar to a DDR bus.
  - Mobile Phones do not need compliance logo, unlike USB/SATA devices.

- No two MIPI devices are the same
  - Variable Data Rates
  - Up to 4 lanes of Data traffic,
  - Multiple different data formats
  - Specification enables custom limits.

- Characterization is significantly important
  - Mobile OEMs select the suppliers based on characterization reports.

Test Equipment & Setups need to be Very Flexible
D-PHY Tx : Opt.D-PHYTX Conformance Test Solution

  - TekExpress option for Fully-Automated testing
  - Provides Conformance and Characterization Testing
  - Based on D-PHY Base Spec v1.0 and UNH’s Conformance Test Suite v0.98.
  - Runs on 7K/C and 70K/B/C scopes

- **Opt.TEKEXP is Pre-Requisite**

- **Differentiation**
  - **Un-parallel Automation**
    - Using Automatic cursor finding of Test Regions
  - **100% Widest Test Coverage**
  - For Conformance testing to Latest CTS (v0.98)
  - Based on Latest Base spec (v1.0)
  - Fully-Automated Temperature Chamber testing

- **Value proposition**
  - Custom-limits/ Limits-Editing on the fly
  - Test Reports
    - Pass/Fail Summary with Margin details & Zoom-in waveform captures
  - Tek 3.5GHz scope is the minimal configuration for accurate testing
## D-PHY Tx : Opt.D-PHYTX Conformance Test Solution Features & Benefits

<table>
<thead>
<tr>
<th>Feature</th>
<th>Benefit</th>
</tr>
</thead>
</table>
| Unparallel-Automated Testing     | • Performs Single-button Fully-Automated testing for set of Transmitter measurements  
                                 | • Enables designers to test devices faster                               |
| Comprehensive Tests coverage     | • 100% Coverage  
                                 | • 49 out of 49 total CTS tests                                          |
| Fully-Automated Temperature Chamber testing | • Validate All High Speed tests using differential probes, Socket XL cables, High-Temperature Tips and Standard Filter Files. |
| Clock Continuous mode            | • Allows selective tests run in Clock Continuous mode                   |
| Escape mode                      | • Allows to perform ULPS &Normal Mode tests                             |
| Characterization/ Margin Testing | • Allows custom-limits or limits-editing to perform Margin testing.  
                                 | • Performs characterization of your design.                             |
| Detailed Test-Reports            | • Provides Pass/Fail summary table, margin details on each test, and waveform screenshot of the testing region for each test. |
D-PHY Tx : Opt.D-PHY Debug and Analysis Solution

  - DPOJET option for Setup Library & MOI
  - Provides **Debug Analysis and Characterization Testing**
  - Based on D-PHY Base Spec v0.9 and UNH’s Conformance Test Suite v0.08.
  - Runs on 7K/C and 70K/B/C scopes

- **Opt.DJA is Pre-Requisite**

- **Differentiation**
  - Flexible for Debug Analysis & Characterization
  - Breadth of Tests Coverage

- **Value proposition**
  - DPOJET Detailed Test Reports
  - DPOJET Scalable for early start on M-PHY (Next Generation Standard)
  - Tek 3.5GHz scope is the minimal configuration for accurate testing
D-PHY Tx : Recommended Test Setup

www.tek.com/applications/computing/serial/recommended_equipment.html#mipi

- **Scope**
  - Recommend: DPO7354/C or DPO/DSA/MSO70404/B/C or higher for risetime accuracies.

- **Probes**
  - For 7Ks: 4x TAPxx/ P6245/ P6249, or 3x TDP3500
  - For 70Ks: 4x P7240 or 3x P73xx with 020-3035-00 tips/ 3x P75xx.

- **Scope Software**
  - Opt.D-PHYTX on TEKEXP For Conformance Test
  - Opt.D-PHY on DPOJET for Debug, Analysis & Characterization
## Tek D-PHY TX and UNH-IOL DPHYGUI Results Correlations

<table>
<thead>
<tr>
<th>Measurement name</th>
<th>Tek Result</th>
<th>UNH Result</th>
<th>Deviation in %</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Dp</td>
<td>Dn</td>
<td>Unit</td>
</tr>
<tr>
<td>Data Lane LP-TX Thevenin Output High Level Voltage (VOH)</td>
<td>1.212</td>
<td>1.209 V</td>
<td>1.212</td>
</tr>
<tr>
<td>Data Lane LP-TX Thevenin Output Low Level Voltage (VOL)</td>
<td>0.024</td>
<td>0.021 V</td>
<td>0.024</td>
</tr>
<tr>
<td>Data Lane Rise Time</td>
<td>24.35</td>
<td>23.89 ns</td>
<td>28.06</td>
</tr>
<tr>
<td>Data Lane Fall Time</td>
<td>14</td>
<td>13.52 ns</td>
<td>13.97</td>
</tr>
<tr>
<td>Clock Lane LP-TX Thevenin Output High Level Voltage (VOH)</td>
<td>1.191</td>
<td>1.209 V</td>
<td>1.191</td>
</tr>
<tr>
<td>Clock Lane LP-TX Thevenin Output Low Level Voltage (VOL)</td>
<td>0.009</td>
<td>0.045 V</td>
<td>0.219</td>
</tr>
<tr>
<td>Clock Lane Rise Time</td>
<td>22.92</td>
<td>22.2 ns</td>
<td>22.83</td>
</tr>
<tr>
<td>Clock Lane Fall Time</td>
<td>14.2</td>
<td>10.68 ns</td>
<td>14.42</td>
</tr>
<tr>
<td>Data Lane HS Entry: Data Lane TLPX Value</td>
<td>70.08 V</td>
<td>70.1</td>
<td>0.0</td>
</tr>
<tr>
<td>Data Lane HS Entry: THS-PREPARE Value</td>
<td>72.32 V</td>
<td>72.4</td>
<td>-0.1</td>
</tr>
<tr>
<td>Data Lane HS Entry: THS-PREPARE + THS-ZERO Value</td>
<td>178.88 ns</td>
<td>178.97</td>
<td>0.0</td>
</tr>
<tr>
<td>Data Lane HS-TX Differential Voltages (V_{DIFF}, V_{OVD})</td>
<td>-211.8</td>
<td>217.2 mV</td>
<td>-214.8</td>
</tr>
<tr>
<td>Clock Lane HS-TX Differential Voltage Mismatch (\Delta V_{DIFF})</td>
<td>5.6 mV</td>
<td>3.5</td>
<td>37.3</td>
</tr>
<tr>
<td>Clock Lane HS-TX Single Ended Output High Voltages (V_{OH}, V_{OH</td>
<td>Z})</td>
<td>455.45 mV</td>
<td>475.47</td>
</tr>
<tr>
<td>Clock Lane HS-TX Common-Mode Voltages (V_{CM}, V_{CM})</td>
<td>395.96</td>
<td>306.78 mV</td>
<td>305.2</td>
</tr>
<tr>
<td>Clock Lane HS-TX Common-Mode Voltage Mismatch (\Delta V_{CM})</td>
<td>0.408 mV</td>
<td>0.7</td>
<td>-71.6</td>
</tr>
<tr>
<td>Clock Lane HS-TX Dynamic Common-Level Variations Between 50-</td>
<td>13.59 mVPK</td>
<td>14.3</td>
<td>-5.2</td>
</tr>
<tr>
<td>Clock Lane HS-TX Dynamic Common-Level Variations Above 450MHz</td>
<td>7 mVrms</td>
<td>7</td>
<td>0.0</td>
</tr>
<tr>
<td>Clock Lane HS-TX 20%-80% Rise time (\tau)</td>
<td>223.6 ns</td>
<td>223.5</td>
<td>0.0</td>
</tr>
<tr>
<td>Clock Lane HS-TX 80%-20% Fall time (\tau)</td>
<td>229.5 ns</td>
<td>229.6</td>
<td>0.0</td>
</tr>
<tr>
<td>Clock Lane HS Exit T_{TR</td>
<td>I} Value</td>
<td>82.45 ns</td>
<td>82.34</td>
</tr>
<tr>
<td>Clock Lane HS Exit 30%-80% Post-EOT Rise Time(T_{R</td>
<td>I</td>
<td>T}) Value</td>
<td>17.04 ns</td>
</tr>
<tr>
<td>Clock Lane HS Entry: T_{PEX} Value</td>
<td>71.28 ns</td>
<td>71.25</td>
<td>0.0</td>
</tr>
<tr>
<td>Clock Lane HS Entry: T_{CM</td>
<td>PREPARE} Value</td>
<td>51.9 ns</td>
<td>50.26</td>
</tr>
<tr>
<td>Clock Lane HS Entry: T_{CM</td>
<td>PREPARE} + T_{ZERO} Value</td>
<td>294.56 ns</td>
<td>293.81</td>
</tr>
<tr>
<td>Clock Lane HS-TX Differential Voltages (V_{DIFF}, V_{OVD})</td>
<td>-188.31</td>
<td>136.39 mV</td>
<td>-184.7</td>
</tr>
<tr>
<td>Clock Lane HS-TX Differential Voltage Mismatch (\Delta V_{DIFF})</td>
<td>51.33 mV</td>
<td>58.2</td>
<td>-13.4</td>
</tr>
<tr>
<td>Clock Lane HS-TX Single Ended Output High Voltages (V_{OH}, V_{OH</td>
<td>Z})</td>
<td>447</td>
<td>471.1</td>
</tr>
<tr>
<td>Clock Lane HS-TX Common-Mode Voltages (V_{CM</td>
<td>I}, V_{CM</td>
<td>O})</td>
<td>314.08</td>
</tr>
<tr>
<td>Clock Lane HS-TX Common-Mode Voltage Mismatch (\Delta V_{CM})</td>
<td>1.61 mV</td>
<td>1.6</td>
<td>0.6</td>
</tr>
<tr>
<td>Clock Lane HS-TX Dynamic Common-Level Variations Between 50-</td>
<td>17.3 mVPK</td>
<td>12.2</td>
<td>29.5</td>
</tr>
<tr>
<td>Clock Lane HS-TX Dynamic Common-Level Variations Above 450MHz</td>
<td>7.46 mVrms</td>
<td>7.4</td>
<td>0.8</td>
</tr>
<tr>
<td>Clock Lane HS-TX 20%-80% Rise time (\tau)</td>
<td>277.3 ns</td>
<td>263.2</td>
<td>5.1</td>
</tr>
<tr>
<td>Clock Lane HS-TX 80%-20% Fall time (\tau)</td>
<td>275.39 ns</td>
<td>258.3</td>
<td>6.2</td>
</tr>
<tr>
<td>Clock Lane HS Exit T_{TR</td>
<td>I} Value</td>
<td>693.87 ns</td>
<td>52.97</td>
</tr>
<tr>
<td>Clock Lane HS Exit 30%-80% Post-EOT Rise Time(T_{R</td>
<td>I</td>
<td>T}) Value</td>
<td>17 ns</td>
</tr>
<tr>
<td>Clock Lane HS Clock Instantaneous (UI_{MAX})</td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>1.134</td>
<td>1.38</td>
<td>NA</td>
<td>1.356</td>
</tr>
<tr>
<td>Mean</td>
<td>1.265</td>
<td>Mean</td>
<td>1.25</td>
</tr>
<tr>
<td>HS Entry T_{CM</td>
<td>PREPARE} Value</td>
<td>67.28 ns</td>
<td>69.3</td>
</tr>
<tr>
<td>HS Exit T_{CM</td>
<td>PREPARE} Value</td>
<td>10361.52 ns</td>
<td>10297.77</td>
</tr>
</tbody>
</table>

Setup: MSO 20GHz scope, 4x P6248 probes, Termination board and probing board from UNH.

* As LP HS waveform is used in this use-case, Tek algorithm finds the LP-00 region and computes VOL in that region, whereas the UNH algorithm considers the LP-00 and HS region for computing VOL. If LP signal is used, the same measurement has 100% correlation.
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DSI/CSI Decode (New)
Probe using Analog, Digital or Mixed Channels
DSI/CSI Decode (New)
Mix of Analog and Digital Channels

- Analog Clock, Digital Data
- Digital Clock, Analog Data

- Flexible, high performance MSO channels allow simultaneous probing of DSI and CSI buses
- Working on multi-lane solution, MSO70k is the only product on the market that could do this
DSI/CSI Decode (New)

Errors indicated in bus decode waveform

- Missing Sync
- Checksum Error
- ECC error

Errors and Warnings indicated in event table
DSI/CSI Decode (New)
Zoom on a row of pixels

- Decoded items:
  - Start of Transmission (SoT)
  - Data Type - Packed Pixel 888
  - Virtual Channel-0, Word Count-60
  - ECC – 07h
  - 1st Pixel Value: Red – 255, Green – 216, Blue – 000
  - All of the pixel values as you scroll
  - Checksum field
  - End of Transmission D-PHY fields
DSI/CSI Decode (New)

Event Table

- Event table lists,
  - Timestamps for each event
  - Short / Long packet indication
  - Data Type, Virtual Channel, Packet Data, Word Count, ECC and Checksum all decoded
  - Number of pixels
  - Error/Warning column indicates problems (this demo signal doesn’t have any)
  - All the data in this long packet is now shown with each pixel labeled and the R, G, and B values for each pixel shown
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D-PHY Rx : Test Solution Overview

- 100% Complete solution for D-PHY Compliance testing
  - Meets all the requirements in UNH-IOL document (v0.98)
  - PG3A is only 4 channel solution available

- System set up is quick and easy
  - No complex VXI system, just stand alone instruments, a probe and a coupler

- Cost effective solution
  - Approx 66% lower list price than competition

- No extra equipment required for protocol testing
  - PG3A is only 4 channel solution for complete CSI and DSI protocol testing

- PG3A Pattern Generator provides
  - Controls clock and signaling to establish link with DUT
  - Adjusts voltage levels, packet type, etc to stress test receiver

- AWG7082C Arbitrary Waveform Generator
  - Adds jitter and interference to the D-PHY signals

Diagram:

- PG3A Pattern Generator
  - Controls clock and signaling
  - Adjusts voltage levels, etc

- AWG7082C Arbitrary Waveform Generator
  - Adds jitter and interference

- D-PHY Coupler
  - Connects PG3A and AWG7082C to DUT

- P332 Probe
  - Connects to PG3A for testing
# D-PHY Rx: Recommended Test Setup

<table>
<thead>
<tr>
<th>Product</th>
<th>Description</th>
<th>Supplier</th>
</tr>
</thead>
<tbody>
<tr>
<td>PG3ACAB*</td>
<td>Pattern Generator</td>
<td>Moving Pixel</td>
</tr>
<tr>
<td>P332*</td>
<td>4 Lane - 1Gb/s Serial Probe for PG3A</td>
<td>Moving Pixel</td>
</tr>
<tr>
<td>PGRemote Software*</td>
<td>Push-button GUI for Creation of D-PHY, CSI2 and DSI signals</td>
<td>Moving Pixel</td>
</tr>
<tr>
<td>AWG7082C</td>
<td>8GS/s, 2 Channel AWG</td>
<td>Tektronix</td>
</tr>
<tr>
<td>D-PHY Coupler</td>
<td>Impedance Matched Couplers for PG3A and AWG7082C</td>
<td>Moving Pixel</td>
</tr>
</tbody>
</table>

* These products are available to purchase directly from Tektronix
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What is M-PHY?

- M-PHY is a flexible architecture that allows the implementer to support high data rates at minimal power, cost & I/O redesign, for applications such as High Definition Video.

- A Fast, Scalable, Serial Communications Architecture
  - Link – Connects M-PHY Transmitter to an M-PHY Receiver
  - Sub-link – Manage one or more lanes
  - Lane – Operation defined in the protocol (DSI, CSI, UniPro, DigRF)
M-PHY Family

source: www.synopsys.com
M-PHY Testing Challenges

<table>
<thead>
<tr>
<th>Signaling Mode</th>
<th>Speed</th>
<th>Level (V)</th>
<th>Impedance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPHY-PWM</td>
<td>576Mbps</td>
<td>500e-3/250e-3</td>
<td>10k/50 ohms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>260e-3/130e-3</td>
<td></td>
</tr>
<tr>
<td>MPHY-SYS</td>
<td>576Mbps</td>
<td>500e-3/250e-3</td>
<td>10k/50 ohms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>260e-3/130e-3</td>
<td></td>
</tr>
<tr>
<td>MPHY-HS</td>
<td>5.83Gbps</td>
<td>250e-3/130e-3</td>
<td>50 ohms</td>
</tr>
</tbody>
</table>

- Higher data rate will increase importance of Signal Integrity of links
  - Acquisition capability of oscilloscope will need to increase
  - More emphasis on timing/jitter and noise (signal integrity)
  - Receiver testing will be needed to stress-test resulting BER

- Termination
  - Two types of terminations - Restive terminated, and not Terminated.
  - LS mode can operate either terminated or not terminated
  - HS mode it is always terminated, so the swing are halved.
Tektronix M-PHY Testing Solution

- Tektronix is **Industry 1st** tools for M-PHY measurements & Decode
  - Announced in September 2010, during MIPI Conference in Athens
- Tek is only tools available today for M-PHY Measurements & Decode
- PSD (Power Spectral Density) measurements are uniquely supported

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Press Release

**Tektronix Introduces Industry’s First Test Tools for MIPI M-PHY Debug and Validation**

**Monday, September 27, 2010**

**Support for New High-Speed M-PHY Specification Includes DPOJET toolset, and M-PHY DigRFv4 Decode for Tektronix Oscilloscopes**

BEAVERTON, OR—(Marketwire - 09/27/10) - Tektronix, Inc., the world’s leading manufacturer of oscilloscopes, today introduced the industry’s first testing tools for the MIPI Alliance M-PHY standard, allowing customers to immediately get started with performance verification and debug for this important new specification using Tektronix DPOJET® and DigRF®v4 Series oscilloscopes.

The announcement was made in conjunction with the MIPI Alliance All-Members meeting taking place this week in Athens, Greece. The M-PHY specification is an essential part of the MIPI Alliance’s vision for more efficient high-speed interfaces on mobile devices. Compared to the current D-PHY specification, M-PHY supports faster chip-to-chip connections while addressing EMI and power dissipation concerns. By moving quickly to offer M-PHY testing tools, Tektronix is stepping up to help ensure rapid delivery of next-generation mobile devices incorporating M-PHY at the physical layer.

*As an active MIPI contributor, Tektronix brings its test and measurement knowledge to the organization, spurring the adoption of D-PHY and M-PHY specifications,* said Joel Hubaux, chairman of the MIPI Alliance. “Tektronix is aiding the adoption of the new M-PHY interface by giving designers the testing tools they need to ensure signal integrity and verify performance of increasingly complex designs.”

Based on the newly ratified MIPI Alliance M-PHY specification, the new Tektronix M-PHY test offering includes a setup library for the popular DPOJET® RF analysis software and methods of implementation (MOSI) developed in close cooperation with UNISYS®. The solution also includes pre- and post-decoding support from Tektronix partner, The Moving Fuel Company, as well as M-PHY DigRF®v4 decode and verification.
New M-PHYTX : M-PHY Automated Testing Solution
Agenda

- MIPI® Standards Overview
- Tek Strategic Involvement in MIPI
- D-Phy testing
  - Tx, & CSI-DSI Decode
  - Rx
- M-Phy testing
  - Tx, & Decode
  - Rx
- DSI &CSI testing - Stimulus
- DSI &CSI testing - Protocol Validation
- SLIMbus &H.S.I testing
- DigRF testing
- Summary, Q&A
M-PHY Rx: Jitter Tolerance Test Solution

- **PWM** (Pulse-Width Modulation) signaling is Uniquely supported by AWGs today for all gears
- **Single-AWG** unit supports both MIPI M-PHY and USB3.

### M-PHY Rx - CTS tests Coverage Available Today

- Differential Input Voltage Amplitude Tolerance (VDIF-RX)
- Receiver Eye Opening and Accumulated Differential Input Voltage (TEYE-RX, VDIF-ACC-RX)
- Common-Mode Input Voltage Tolerance (VCM-RX) 22
- Receiver Jitter Tolerance (TJRX, SJRX, RJRX, STTJRX, STSJRX)
- Receiver Pulse Width Tolerance (TPULSE-RX)
M-PHY Rx : Error Detector Test Solution
BER on scope using Opt.ERRDT

- **8B/10B Data:**
  - Hardware Serial trigger: 1.25 Gb/s to 6.25 Gb/s
  - BER (Opt.ERRDT): Covers all the above data rate range
M-PHY Tx & Rx Recommended Test Setup

www.tek.com/applications/computing/serial/recommended_equipment.html#mipi

- Oscilloscopes
  - DPO70604/B/C for HS-GEAR1
  - DPO70804/B/C or above for GEAR1/2
  - DPO72004/B/C or above for All GEARs

- Probes
  - 2x P73xx/P73xxSMA (up to HS-Gear2),
    or 2x P75xx with P75LRST tip (up to HS-Gear3) for HS.
  - 2x P73xx/P73xxSMA for PWM (All Gears)

- Signal Generators for Rx
  - AWG7122C with Option #6.

- Software
  - New Opt.M-PHYTX based on DPOJET
  - MPHYVIEW, for DigRFv4 Protocol Decode.
  - Opt.SR-810B, for 8b/10b Serial Analysis.
  - Optional: ERRDT Scope Error Detector
  - Optional: SerialXpress Software for AWG.

- Fixtures
  - No Fixtures required as MIPI/ M-PHY is a chip-to-chip interface with live Master-Slave / Receiver-end connected.
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Stimulus

- **Protocol Testing** – Stimulating buses with known good data packets or packets with intentional errors tests the system’s adherence to a specified protocol.

- **Infrequent Events** - System bugs that only appear when infrequent events occur can be quickly reproduced with a pattern generator by repeatedly stimulating the system with the key external event.

- **Automated Test** – Production line test setups can utilize the PG3A as a general purpose digital I/O source with a large number of channels.
P332 MIPI D-PHY Probe

Key Features

- MIPI D-PHY Probe for use with PG3AMOD and PG3ACAB
- Generate CSI2 and DSI data over D-PHY
- 4-Data Lanes and 1-Clock lane
- 1Gbps (P331) or 1.5Gbps (P332) / Lane data rate
- SMA outputs for each lane
- LP and HS Voltage and Timing adjustable on a each lane separately

Preserve your investment with the ONLY 4 lane, 1.5Gbps stimulus solution in the market.
Stimulus Setup

TLA or PC

PGRemote → PGApp

USB

Inputs Probe

Master Clock

P332

DUT

CSI2 or DSI over D-PHY
PGRemote
Push Button Interface to generate CSI2 / DSI Vectors

PGRemote Main Window

- Command Buttons
- PG, probe status and operational controls
- Status Bar
- Configuration Parameters for PG playback, and D-PHY
- Define CSI/DSI commands and arguments

Oscilloscope Fundamentals - © 2011 Tektronix
PGRemote

- Push Button User interface to generate CSI2 or DSI vectors and probe control
- Real-time adjustment of frequency, voltage and delay in HS and LP modes
- Ability to adjust D-PHY state timing parameters
- Ability to adjust frame timing and generate looping video
- Enter and exit Low power states
- Create custom commands, Macros and assign them to buttons
- Save restore a configuration
- Ability to use P331 as a generic high-speed serial probe
- Demo for free, License required to run with hardware
- The PG can be operated in several modes
  - Pushbutton Mode using the PGRemote software
  - Macro Mode using the PGRemote software
  - Scripting
  - Full remote control mode
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- Summary, Q&A
Requirements of the DigRF Test Bench

- **BBIC**
  - Physical Layer Analysis
  - Stimulus with ideal and non ideal signals
  - Analysis of DigRF protocol and IQ data
  - Analysis DSP and uP

- **RFIC**
  - Physical Layer Analysis
  - Stimulus with ideal and non ideal signals
  - Analysis of DigRF protocol and IQ data
  - RF & Modulation Analysis

- **Integration**
  - Physical Layer Analysis
  - Correlated analysis from DSP to DigRF to RF
Analysis – DigRF Verification & Debug

- No specialized hardware or probing is required

- Minimum impact on signal integrity
  - Simultaneous digital and analog acquisition w/ single probe

- Flexible data extraction for complete analysis
  - Extract IQ data for Modulation Analysis
  - Extract sync, header & payload data

- Customizable S/W, allowing propriety and non compliant DigRF signals to acquired and analyzed

- DigRF solution is available free-of-charge
Analysis – Signal Integrity

- DPOJET Jitter and Timing Analysis Software provide the highest accuracy and lowest noise jitter measurements available.

- Identifies rare anomalies or glitches in seconds with Real-Time DPO acquisition.

- Most complete trigger system in the industry.

- User customizable User Interface.
Analysis - RF

- Live RF spectrum display for transient and spectrum occupancy evaluation
- Trigger on signals other analyzers miss
- Capture and Analyze modulation and frequency switching transients
- 110MHz Real-time BW w/ -73dBc SFDR
- Correlated windows for easy fault identification
Tektronix’ DigRF Solution
Complete solution from Baseband to RF

- Complete solution using industry leading test equipment
  - AWG5000 for Signal Generation
  - TLA7012 for DigRF & Digital Analysis
  - DPO7000 for Signal Integrity issues
  - RTSA for RF and Modulation Analysis

- DigRF Physical Layer & Protocol analysis on logic analyzer without using specialized external hardware
  - Standard probes acquire the signal
  - DigRF Application software processes the data

- Flexibility to generate and analysis ideal, non-ideal and propriety versions of DigRF
  - DigRF Application is customizable by the user
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Summary - Tektronix MIPI Solutions
Single scalable-setup for both D-PHY & M-PHY

Optimal MIPI Configuration:

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
<th>Qty</th>
<th>D-PHY</th>
<th>M-PHY</th>
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<td>12.5 GHz Digital Serial Analyzer; 4 analog channels</td>
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<td>SolderIn Tips for P73xx probes for MIPI</td>
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<td>MPHYVIEW</td>
<td>M-Phy - Digital RF software</td>
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<td>P331</td>
<td>Moving Pixel - 1Gbs Serial Probe for PG3A</td>
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<td>PGRremote-CSI/DSI</td>
<td>Moving Pixel - PG3A generation of CSI or DSI signals</td>
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<td>D-PHY Coupler Set</td>
<td>AWG / PG3A Coupler Set (Not on Tek price list yet)</td>
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<td>SDX100</td>
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<td>Serial Pattern triggering up to 6.25Gb/s</td>
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</tbody>
</table>
Additional References

www.tek.com/applications/computing/serial/recommended_equipment.html#mipi

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**www.Tek.com/MIPI**:  
- **D-PHY Datasheet**  
- **D-PHY/CSI/DSI Application Note**  
- **DigRF Application Note**  
- **MIPI Fact Sheet**:  
- **Opt. M-PHY MOI**  
- **Opt. D-PHY MOI**  
- **MPHYVIEW DigRFv4 Decode Datasheet & Manual**  
  - [http://www.movingpixel.com/MIPI_MPhy.html#MIPI_MVu](http://www.movingpixel.com/MIPI_MPhy.html#MIPI_MVu)  

**Other:**  
- **MIPI Alliance Video on Tek Solutions**  
  - [http://www.youtube.com/watch?v=Mf9rvX2YG4&feature=channel](http://www.youtube.com/watch?v=Mf9rvX2YG4&feature=channel)
Thank you