MIPI DigRF 3G and MIPI DigRF v4 Solutions in Action

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Synopsys

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Agenda

• MIPI DigRF Introduction
• MIPI DigRF 3G / v4 Spec Comparison
• Typical MIPI DigRF v4 Implementations
• MIPI DigRF 3G Solution
• MIPI DigRF v4 Solution
• MIPI DigRF v4 coreConsultant
• MIPI DigRF v4 RFIC Interoperability
• The Industry’s First Silicon-Proven MIPI DigRF v4 M-PHY
• Growing Portfolio of DesignWare® MIPI IP Solutions
MIPI DigRF Introduction

Baseband Processor

DigRF v4 Master  M-PHY

DigRF 3G Master  PHY

4G RF IC

M-PHY  DigRF v4 Slave

2G/3G RF IC

PHY  DigRF 3G Slave

Mobile Terminal
### MIPI DigRF 3G / v4 Spec Comparison

<table>
<thead>
<tr>
<th></th>
<th>DigRF 3G</th>
<th>DigRF v4</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Supported standards</strong></td>
<td>2.5 GPRS/EGPRS with RX diversity</td>
<td>Same as DigRF 3G plus:</td>
</tr>
<tr>
<td></td>
<td>3.5G UMTS with RX diversity</td>
<td>LTE, WiMax, WLAN with RX diversity, MIMO</td>
</tr>
<tr>
<td><strong>PHY</strong></td>
<td>DigRF V3 specific</td>
<td>M-PHY</td>
</tr>
<tr>
<td></td>
<td>- Serial</td>
<td>- Serial</td>
</tr>
<tr>
<td></td>
<td>- Source synchronous</td>
<td>- Source synchronous</td>
</tr>
<tr>
<td></td>
<td>- Differential (LVDS)</td>
<td>- Differential (SLVS)</td>
</tr>
<tr>
<td><strong>Max throughput</strong></td>
<td>- 312 Mbps</td>
<td>- 1456 / 1459.2 Mbps (Mandatory)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- 2912 / 2918.4 Mbps (Optional)</td>
</tr>
<tr>
<td><strong>System clocks (from spec)</strong></td>
<td>19.2, 26.0 and 38.4 MHz</td>
<td>26.0, 38.4 and 52 MHz</td>
</tr>
<tr>
<td><strong>Supported speeds per lane</strong></td>
<td>HS (312Mbps)</td>
<td>HS (1.5Gbps)</td>
</tr>
<tr>
<td></td>
<td>MS (Sysclk)</td>
<td>[3Gbps optional]</td>
</tr>
<tr>
<td></td>
<td>LS (Sysclk/4)</td>
<td>Type II (Sysclk)</td>
</tr>
<tr>
<td><strong>Maximum lane configuration</strong></td>
<td>n.a.</td>
<td>4TX + 4RX</td>
</tr>
<tr>
<td><strong>EMI concerns</strong></td>
<td>Differential signaling</td>
<td>Same as DigRF 3G plus:</td>
</tr>
<tr>
<td></td>
<td>Low amplitude</td>
<td>- Slew rate control</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Different gear/rates</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Dithering</td>
</tr>
<tr>
<td><strong>Line coding</strong></td>
<td>None</td>
<td>8b10b</td>
</tr>
<tr>
<td><strong>PHY protocol interface</strong></td>
<td>Proprietary (at-speed serial interface)</td>
<td>DATA/CTRL SAP</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(1x, 2x, or 4x Symbols wide)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(bitrate/{10, 20, or 40})</td>
</tr>
</tbody>
</table>
Typical MIPI DigRF v4 Implementations

- **No Diversity**
  - Single RFIC with single Rx channel
  - Not a common implementation for LTE
- **Application example: LTE 20MHz**
  - Rx Data rate with overhead: 844.8 Mbps
  - Tx Data rate with overhead: 1013.76 Mbps
- Requires 1 Rx and 1 Tx data paths on DigRF v4 interface

- **Local Diversity**
  - Single RFIC with 2 Receive channels
  - Common implementation for LTE Category 3
- **Application example: LTE 20MHz**
  - Rx Data with overhead: 1689.6 Mbps
  - Tx Data with overhead: 1013.76 Mbps
- Requires 2 Rx and 1 Tx data paths on DigRF v4 interface
MIPI DigRF 3G Solution
Master Controller and PHY

3G DigRF Master Interface

3G DigRF Master Controller
- Payload Processing
- Header Decoding
- Frame Construction
- Serialization
- DigRF Controller FSM
- DigRF Control and Configuration

3G DigRF PHY
- PLL
- Time aligner
- Test Interface

Digital Baseband and DSP
- RX primary FIFO I+Q
- RX diversity FIFO I+Q
- TX FIFO I+Q

AMBA-APB Master Interface

Test Controller

DigRF 3G Line Signals (to RFIC)
- txdatap
- txdatan
- rxdatap
- rxdatan
- sysclk
- sysclkEn
• GUI to guide through design flow activities and configure core to meet baseband requirements
MIPI DigRF v4 RFIC Interoperability
The Industry’s First Silicon-Proven MIPI M-PHY

Watch the video:  

Key Features

- Compliant with latest MIPI M-PHY spec
- Fully integrated hard macro
  - 9 pins for standard 2Rx/1Tx implementation
  - Includes PLL and Biasing block
- Supports M-PHY Type II M-PORT
  - Optimized for DigRF v4
  - Supports all DigRF v4 mandatory features
- Supports High-Speed G1 A/B modes
  - 1.248Gbps & 1.456/1.4592Gbps
- Programmable slew-rate control
- Small and Large amplitudes
A Growing portfolio of DesignWare MIPI IP Solutions

- DigRF 3G controller
- DigRF 3G PHY
- DigRF v4 controller
- M-PHY
- CSI-2 Host controller
- DSI Host controller
- D-PHY

Thank you!

For more information visit www.synopsys.com/mipi