MIPI DigRF 3G and MIPI DigRF v4 Solutions in Action

Luis Laranjeira
Synopsys

Member-to-Member
Presentations
March 9, 2011

Legal Disclaimer

The material contained herein is not a license, either expressly or impliedly, to any IPR owned or controlled by any of the authors or developers of this material or MIPI. The material contained herein is provided on an “AS IS” basis and to the maximum extent permitted by applicable law, this material is provided AS IS AND WITH ALL FAULTS, and the authors and developers of this material and MIPI hereby disclaim all other warranties and conditions, either express, implied or statutory, including, but not limited to, any (if any) implied warranties, duties or conditions of merchantability, of fitness for a particular purpose, of accuracy or completeness of responses, of results, of workmanlike effort, of lack of viruses, and of lack of negligence. ALSO, THERE IS NO WARRANTY OR CONDITION OF TITLE, QUIET ENJOYMENT, QUIET POSSESSION, CORRESPONDENCE TO DESCRIPTION OR NON-INFRINGEMENT WITH REGARD TO THIS MATERIAL.

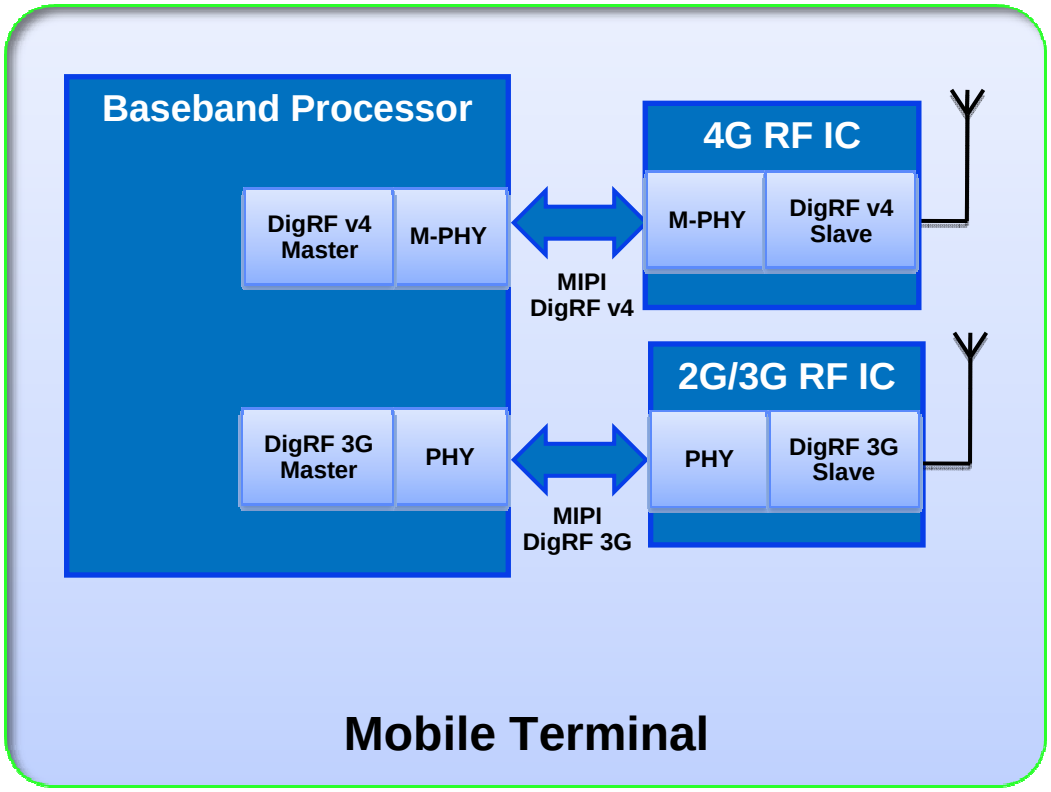
All materials contained herein are protected by copyright laws, and may not be reproduced, republished, distributed, transmitted, displayed, broadcast or otherwise exploited in any manner without the express prior written permission of MIPI Alliance. MIPI, MIPI Alliance and the dotted rainbow arch and all related trademarks, tradenames, and other intellectual property are the exclusive property of MIPI Alliance and cannot be used without its express prior written permission.

IN NO EVENT WILL ANY AUTHOR OR DEVELOPER OF THIS MATERIAL OR MIPI BE LIABLE TO ANY OTHER PARTY FOR THE COST OF PROCURING SUBSTITUTE GOODS OR SERVICES, LOST PROFITS, LOSS OF USE, LOSS OF DATA, OR ANY INCIDENTAL, CONSEQUENTIAL, DIRECT, INDIRECT, OR SPECIAL DAMAGES WHETHER UNDER CONTRACT, TORT, WARRANTY, OR OTHERWISE, ARISING IN ANY WAY OUT OF THIS OR ANY OTHER AGREEMENT RELATING TO THIS MATERIAL, WHETHER OR NOT SUCH PARTY HAD ADVANCE NOTICE OF THE POSSIBILITY OF SUCH DAMAGES.

Agenda

- MIPI DigRF Introduction
- MIPI DigRF 3G / v4 Spec Comparison
- Typical MIPI DigRF v4 Implementations
- MIPI DigRF 3G Solution
- MIPI DigRF v4 Solution
- MIPI DigRF v4 coreConsultant
- MIPI DigRF v4 RFIC Interoperability
- The Industry's First Silicon-Proven MIPI DigRF v4 M-PHY
- Growing Portfolio of DesignWare® MIPI IP Solutions

MIPI DigRF Introduction

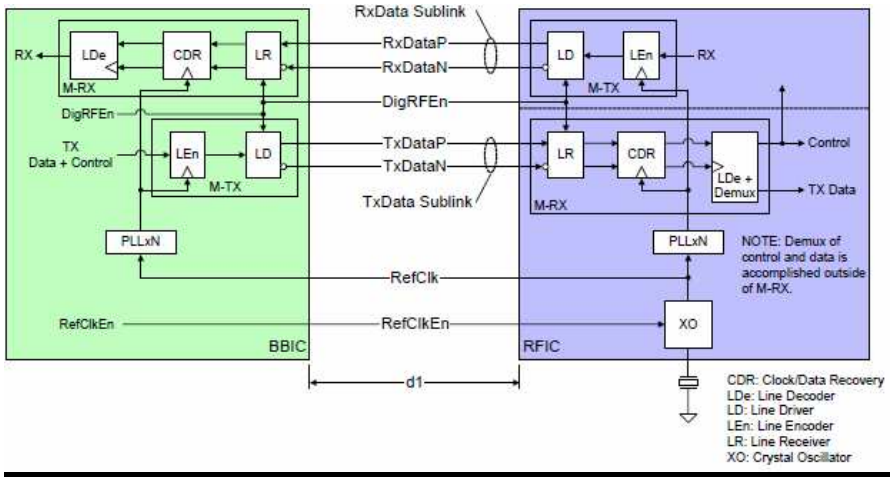


MIPI DigRF 3G / v4 Spec Comparison

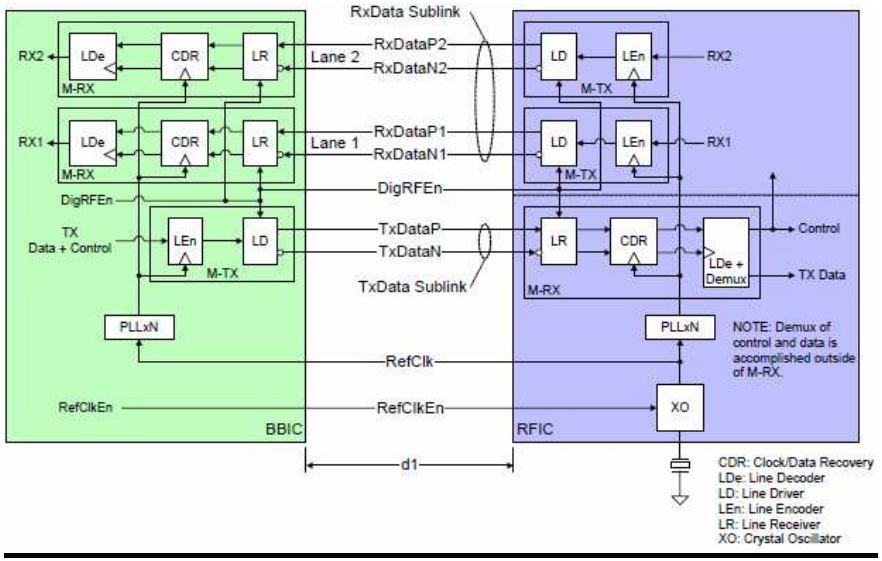
	DigRF 3G	DigRF v4
Supported standards	2.5 GPRS/EGPRS with RX diversity 3.5G UMTS with RX diversity	**Same as DigRF 3G plus:** **LTE, WiMax, WLAN with RX diversity, MIMO**
PHY	DigRF V3 specific -Serial -Source synchronous -Differential (LVDS)	**M-PHY** - Serial - Source synchronous - Differential (SLVS)
Max throughput	- 312 Mbps	- **1456 / 1459.2 Mbps (Mandatory)** - 2912 / 2918.4 Mbps (Optional)
System clocks (from spec)	19.2, 26.0 and 38.4 MHz	26.0, 38.4 and 52 MHz
Supported speeds per lane	HS (312Mbps) MS (Sysclk) LS (Sysclk/4)	HS (1.5Gbps) [3Gbps optional] Type II (Sysclk)
Maximum lane configuration	n.a.	4TX + 4RX
EMI concerns	Differential signaling Low amplitude	**Same as DigRF 3G plus:** **- Slew rate control** **- Different gear/rates** **- Dithering**
Line coding	None	**8b10b**
PHY protocol interface	Proprietary (at-speed serial interface)	**DATA/CTRL SAP** (1x, 2x, or 4x Symbols wide) (bitrate/{10,20, or 40})

Typical MIPI DigRF v4 Implementations

Basic Handset



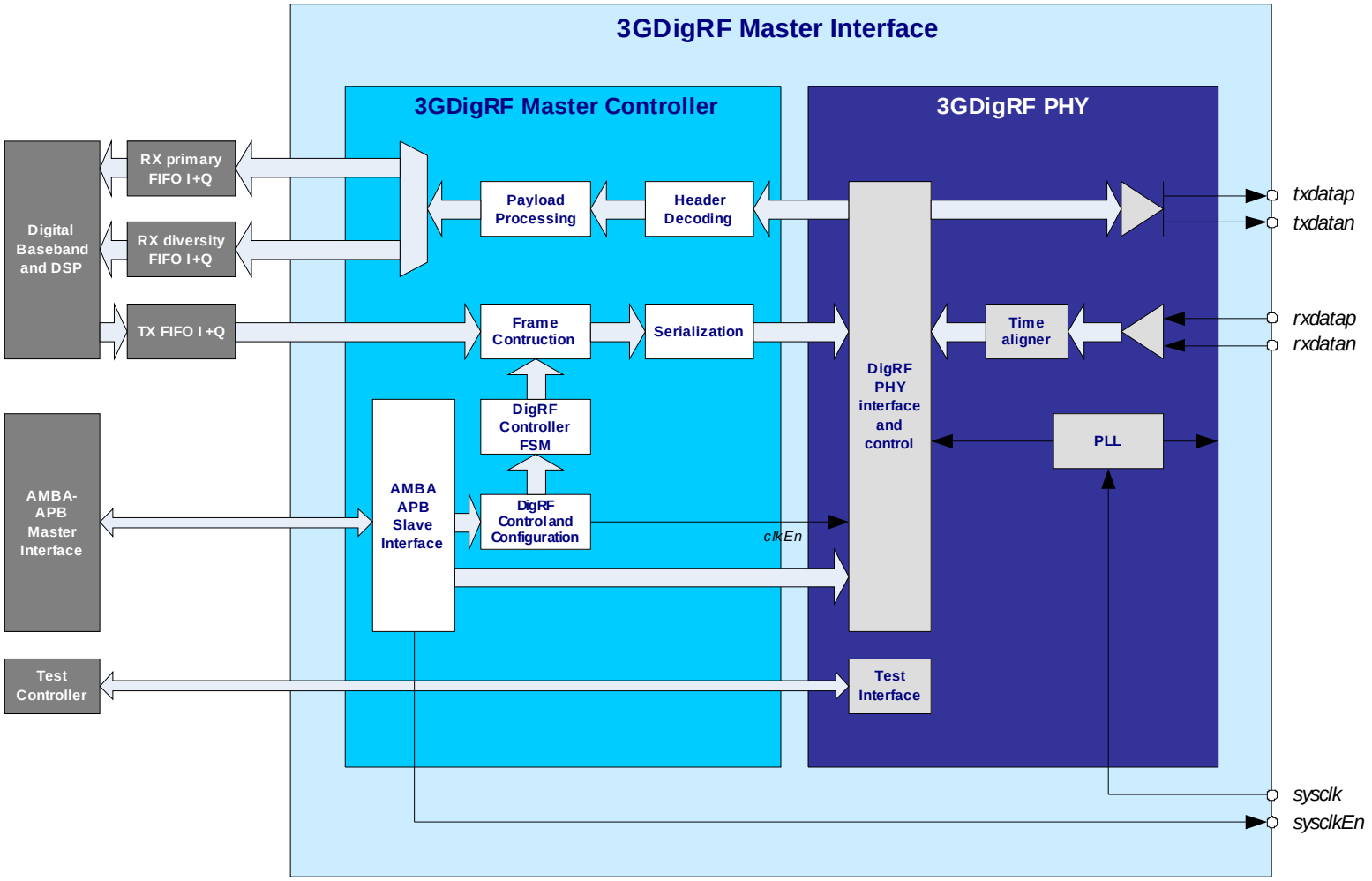
Basic Handset with local Diversity



- No Diversity
  - Single RFIC with single Rx channel
  - Not a common implementation for LTE
- Application example: LTE 20MHz
  - Rx Data rate with overhead: 844.8 Mbps
  - Tx Data rate with overhead: 1013.76 Mbps
- Requires 1 Rx and 1 Tx data paths on DigRF v4 interface

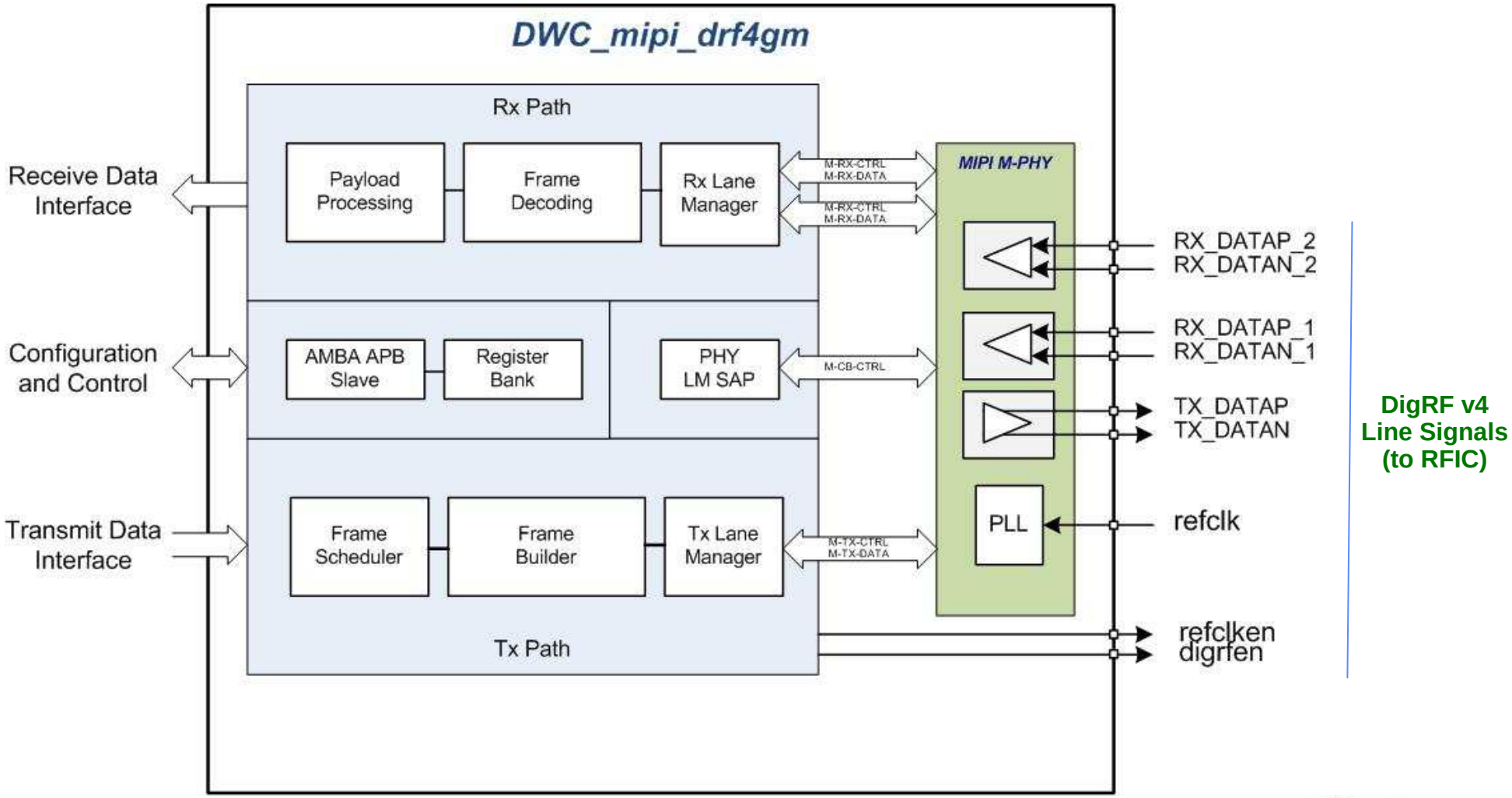
- Local Diversity
  - Single RFIC with 2 Receive channels
  - Common implementation for LTE Category 3
- Application example: LTE 20MHz
  - Rx Data with overhead: 1689.6 Mbps
  - Tx Data with overhead: 1013.76
- Requires 2 Rx and 1 Tx data paths on DigRF v4 interface

MIPI DigRF 3G Solution
Master Controller and PHY

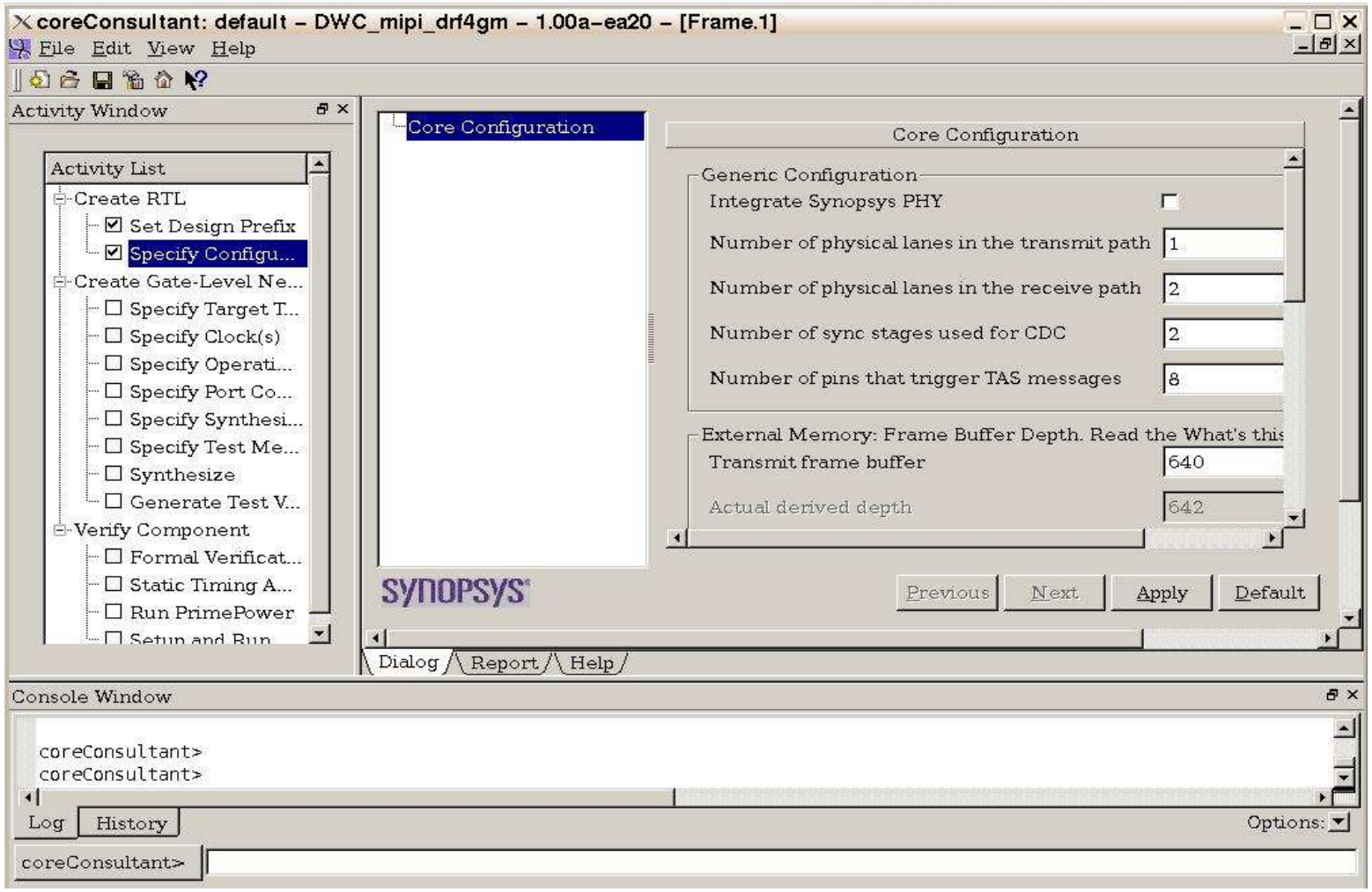


DigRF 3G Line Signals (to RFIC)

MIPI DigRF v4 Solution
Master controller and M-PHY

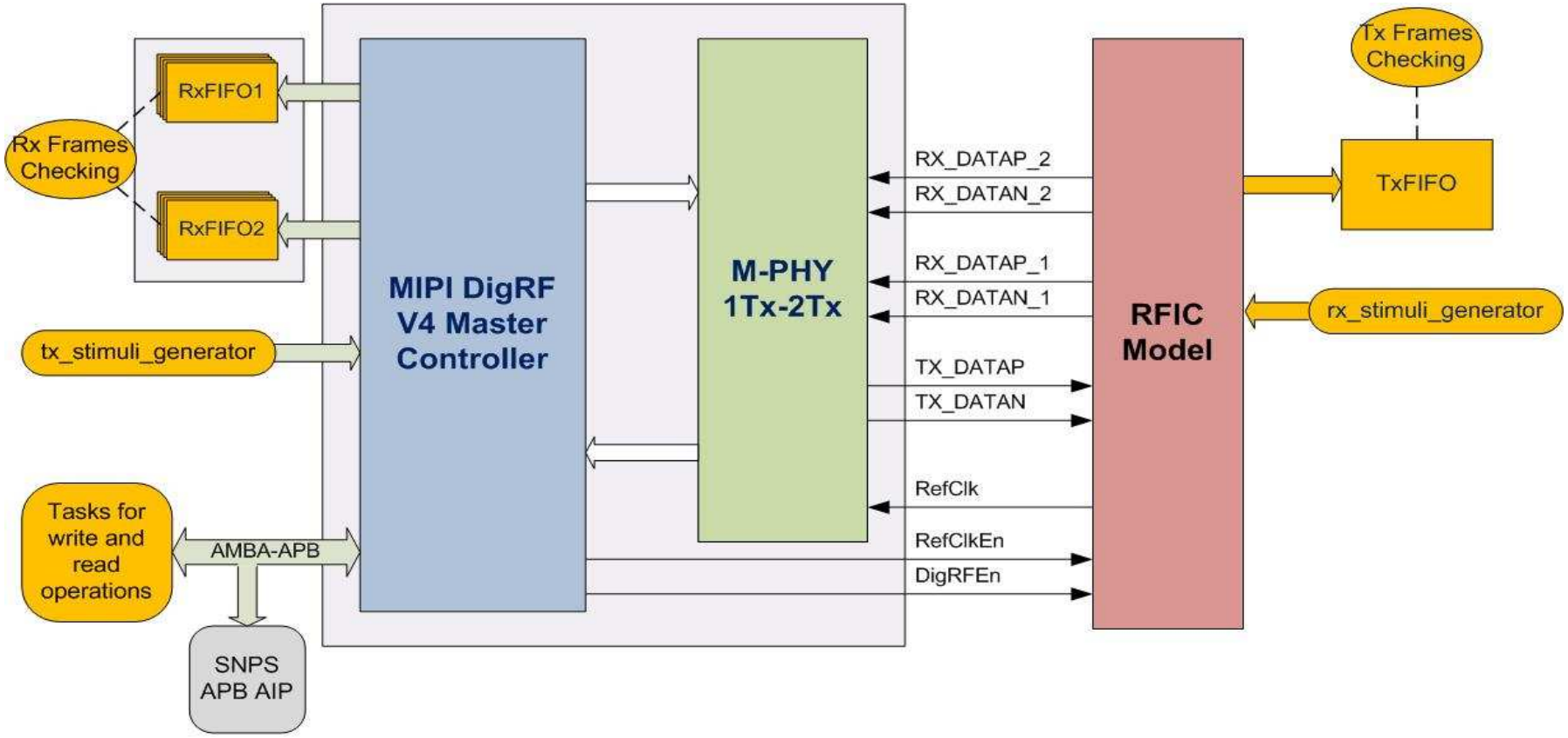


MIPI DigRF v4 coreConsultant



- GUI to guide through design flow activities and configure core to meet baseband requirements

MIPI DigRF v4 RFIC Interoperability

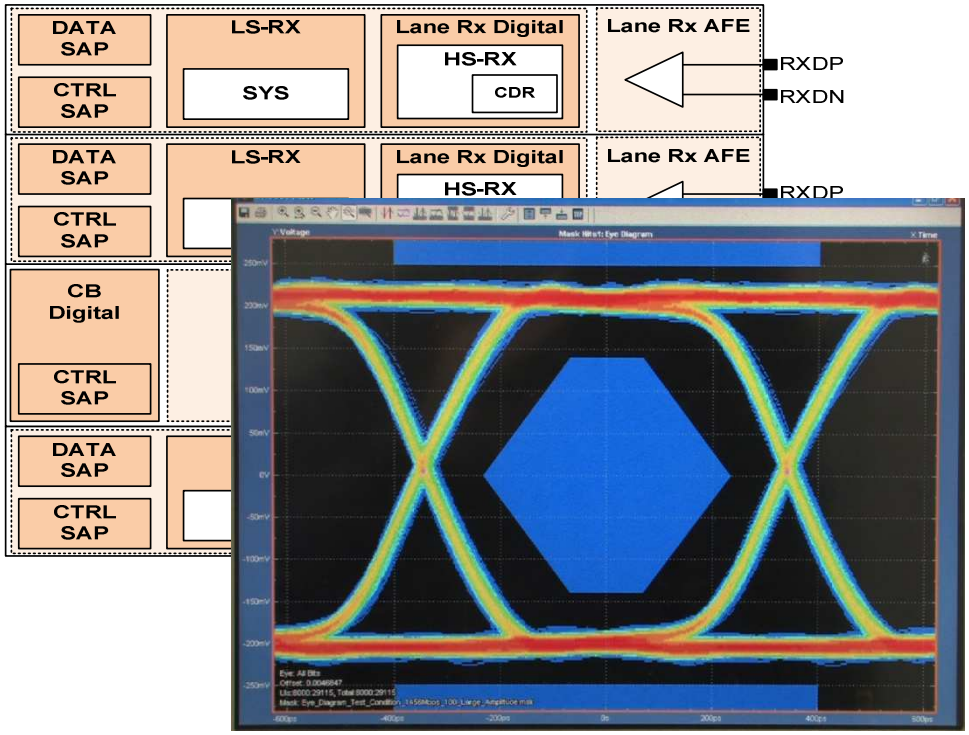


The Industry's First Silicon-Proven MIPI M-PHY

Silicon-Proven

Watch the video:

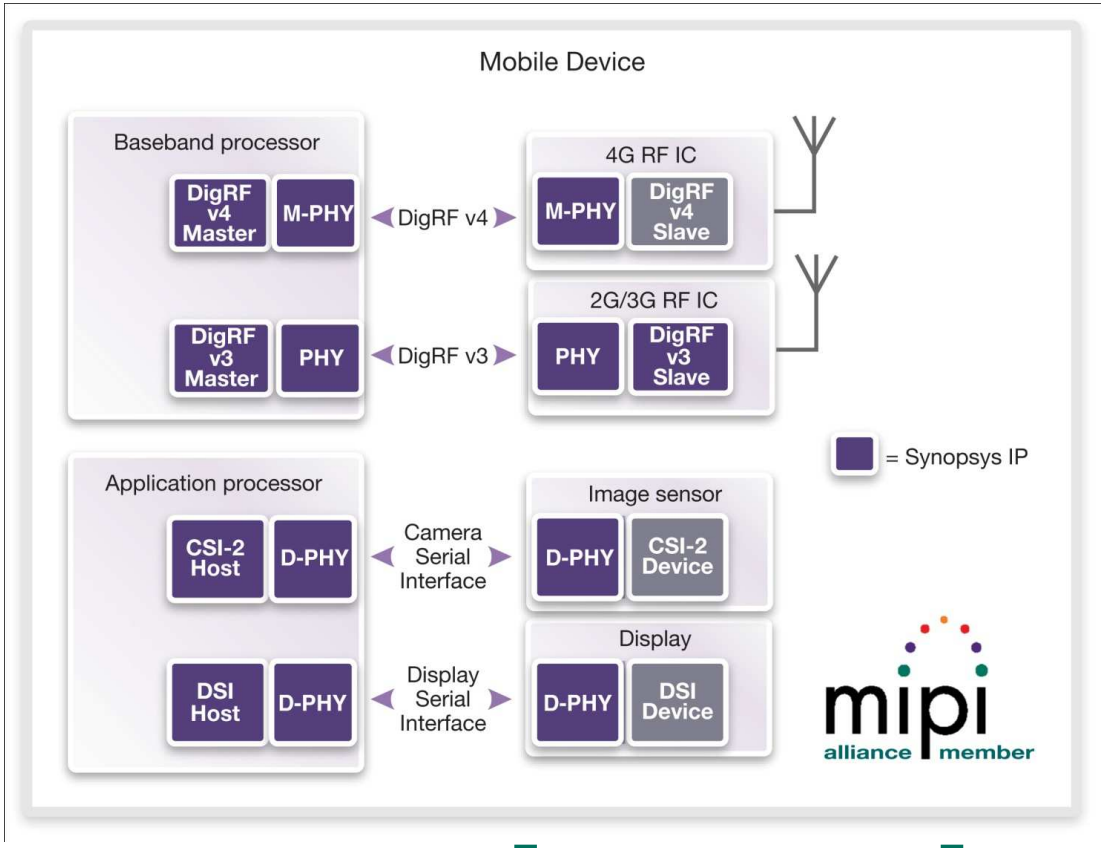
http://www.synopsys.com/dw/ipdir.php?ds=mipi_m-phy



Key Features

- Compliant with latest MIPI M-PHY spec
- Fully integrated hard macro
  - 9 pins for standard 2Rx/1Tx implementation
  - Includes PLL and Biasing block
- Supports M-PHY Type II M-PORT
  - Optimized for DigRF v4
  - Supports all DigRF v4 mandatory features
- Supports High-Speed G1 A/B modes
  - 1.248Gbps & 1.456/1.4592Gbps
- Programmable slew-rate control
- Small and Large amplitudes

A Growing portfolio of DesignWare MIPI IP Solutions



- DigRF 3G controller
- DigRF 3G PHY
- DigRF v4 controller
- M-PHY
- CSI-2 Host controller
- DSI Host controller
- D-PHY

Thank you!

For more information visit **www.synopsys.com/mipi**