



MIPI Alliance Recommendation for Debug and Trace Connectors

Version 1.10.00 – 16 March 2011

MIPI Board Approved for Public Distribution 19-Apr-2011

Further technical changes to this document are expected as work continues in the Debug Working Group

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45 Contents

| | | |
|----|---|----|
| 46 | Version 1.10.00 – 16 March 2011 | i |
| 47 | 1 Overview | 8 |
| 48 | 1.1 Scope | 8 |
| 49 | 1.1.1 Document Is..... | 8 |
| 50 | 1.1.2 Document Is Not..... | 9 |
| 51 | 1.1.3 Related Specifications | 9 |
| 52 | 1.2 Purpose | 9 |
| 53 | 2 Terminology | 10 |
| 54 | 2.1 Definitions | 10 |
| 55 | 2.2 Abbreviations | 10 |
| 56 | 2.3 Acronyms | 10 |
| 57 | 3 References | 11 |
| 58 | 4 Signal Descriptions..... | 12 |
| 59 | 4.1 Reference Voltage Pins | 15 |
| 60 | 4.2 nRESET..... | 15 |
| 61 | 4.3 nTRST_PD and nTRST..... | 16 |
| 62 | 4.3.1 Merging nTRST_PD and nTRST at the Board Level..... | 16 |
| 63 | 4.4 Exclusive Two-Pin IEEE 1149.7..... | 17 |
| 64 | 5 Basic Debug Connector..... | 18 |
| 65 | 5.1 Connector Type | 18 |
| 66 | 5.1.1 Connector Sources | 18 |
| 67 | 5.2 Pin Mapping | 20 |
| 68 | 5.2.1 Rules for Pin Mapping..... | 20 |
| 69 | 5.2.2 Recommended Pin Mappings | 20 |
| 70 | 5.2.3 Physical Orientation of the Connector on the PCB..... | 23 |
| 71 | 5.2.4 Cable-end Design Recommendations | 23 |
| 72 | 6 High Speed Parallel Trace Connectors..... | 24 |
| 73 | 6.1 Recommended HSPT Connector..... | 24 |
| 74 | 6.1.1 PCB Connector..... | 24 |
| 75 | 6.1.2 Cable Connector | 24 |
| 76 | 6.1.3 Connector Options..... | 25 |
| 77 | 6.1.4 Connector Pin Mapping..... | 25 |
| 78 | 6.1.5 Supported Pin Mapping Configurations | 26 |
| 79 | 6.1.6 DTC Support for Multiple PTI Mapping..... | 27 |

| | | | |
|-----|---------|--|----|
| 80 | 6.1.7 | Physical Orientation of the Connector on the PCB..... | 27 |
| 81 | 6.1.8 | Cable-end Design Recommendations..... | 29 |
| 82 | 6.2 | Legacy Connector..... | 29 |
| 83 | 6.2.1 | Legacy Pin Mapping for Wide JTAG and a Single PTI Channel..... | 30 |
| 84 | 7 | Design Considerations..... | 31 |
| 85 | 7.1 | Electrical Recommendations..... | 31 |
| 86 | 7.2 | Signal Buffering..... | 31 |
| 87 | 7.2.1 | Buffering Basic Debug Signals..... | 31 |
| 88 | 7.2.2 | Buffering Trace (PTI) Signals..... | 31 |
| 89 | 7.3 | Debug and Trace Connectors on the Same Target Board..... | 31 |
| 90 | 7.3.1 | Debug Signals to Two Connectors..... | 32 |
| 91 | 7.3.2 | Legacy Trace Connector and Multiple Reference Voltages..... | 32 |
| 92 | 7.4 | TRC_DATA Signal Routing on PCB..... | 32 |
| 93 | 7.5 | Overlaying Multiple PTIs on an ASIC Boundary..... | 32 |
| 94 | 7.5.1 | Simple Shared Interfaces..... | 33 |
| 95 | 7.5.2 | Complex Shared Interfaces..... | 34 |
| 96 | 7.5.3 | ASIC Pin Mapping for Simultaneous Shared Interfaces..... | 34 |
| 97 | 7.5.4 | Connector Mapping for Simultaneous Shared Interfaces..... | 36 |
| 98 | Annex A | Debugger and Target Presence Detection..... | 38 |
| 99 | Annex B | ARM ETM Pin Mapping..... | 40 |
| 100 | B.1 | Standard ETM Pin Mapping..... | 40 |
| 101 | B.2 | Demultiplexed ETM Pin Mapping..... | 41 |
| 102 | B.3 | Multiplexed ETM Pin Mapping..... | 42 |
| 103 | Annex C | Nexus Pin Mapping..... | 44 |

| | | |
|-----|--|----|
| 104 | Figures | |
| 105 | Figure 1 VREF_DEBUG Options | 15 |
| 106 | Figure 2 VREF_TRACE Options | 15 |
| 107 | Figure 3 nRESET Signal Handling | 15 |
| 108 | Figure 4 nTRST and nTRST_PD Merged as nTRST | 17 |
| 109 | Figure 5 nTRST and nTRST_PD Merged as nTRST_PD | 17 |
| 110 | Figure 6 Basic Debug Connector (34-pin)..... | 18 |
| 111 | Figure 7 Basic Debug Orientation on the PCB (34-pin Example)..... | 23 |
| 112 | Figure 8 QSH and QTH Connectors..... | 24 |
| 113 | Figure 9 Cable and Board Clearance Example Showing Improper Board Design Relative to the Clearance 114 Required for Cable-end | 28 |
| 115 | Figure 10 QSH Orientation on the PCB and Low Clearance/Keep-out Area..... | 28 |
| 116 | Figure 11 MICTOR PCB (left) and Cable End Connectors | 29 |
| 117 | Figure 12 Signaling Model for Trace and Other High-speed Pins | 31 |
| 118 | Figure 13 Multiplexed PTIs at the ASIC Level..... | 33 |
| 119 | Figure 14 Example of PTI Signal Overlays at the ASIC Boundary | 37 |
| 120 | Figure 15 Bi-directional Presence Detect | 39 |
| 121 | Figure 16 ASIC Level Multiplexing with, and without, TRACECTL | 41 |

| | | |
|-----|--|----|
| 122 | Tables | |
| 123 | Table 1 Signal Descriptions..... | 13 |
| 124 | Table 2 PCB Mounted Connector Part Number Templates..... | 19 |
| 125 | Table 3 Cable Connector Part Number Templates | 19 |
| 126 | Table 4 MIPI Recommended Pin Mapping for Basic Debug | 21 |
| 127 | Table 5 PCB Mounted Connectors | 24 |
| 128 | Table 6 Cable or DTC Adaptor Connectors | 25 |
| 129 | Table 7 Connector Options..... | 25 |
| 130 | Table 8 QSH/QTH Pin Mapping with a Maximum of 4 PTIs | 25 |
| 131 | Table 9 Multiple Channel Configurations | 27 |
| 132 | Table 10 Legacy (MICTOR) Part Numbers | 29 |
| 133 | Table 11 Legacy MICTOR with JTAG and a 16 Data Signal PTI..... | 30 |
| 134 | Table 12 Simple Multiplexed Pin Mapping..... | 33 |
| 135 | Table 13 Simultaneous Export Pin Mapping | 36 |
| 136 | Table 14 ETMv1/2 to PTI Mapping | 40 |
| 137 | Table 15 ETMv3 to PTI Mapping | 40 |
| 138 | Table 16 ETMv3 to PTI Mapping for Overlay Scenario..... | 41 |
| 139 | Table 17 Demultiplexed ETMv1 to PTI Mapping..... | 41 |
| 140 | Table 18 Demultiplexed ETMv2 to PTI Mapping..... | 42 |
| 141 | Table 19 Multiplexed ETMv1 to PTI Mapping..... | 42 |
| 142 | Table 20 Multiplexed ETMv2 to PTI Mapping..... | 43 |
| 143 | Table 21 Nexus Message Interface to PTI Mapping | 44 |
| 144 | Table 22 Nexus Extended Pin Mapping | 44 |

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Release History

| Date | Release | Description |
|------------|---------|---|
| 2007-06-07 | 1.00.00 | Initial board adopted release. |
| 2011-06-29 | 1.10.00 | Changed name to "MIPI Alliance Recommendation for Debug and Trace Connectors" from "MIPI Alliance Recommendation for Debug: Debug and Trace Connectors". Added keyed connector part numbers for the basic debug connector. Added recommendation for overlaying multiple interfaces on trace channels. |
| 2011-08-30 | 1.10.00 | Board approved release. |

146 MIPI Alliance Recommendation for TDC

147 1 Overview

148 1.1 Scope

149 This document provides a recommendation for board level mating connectors that supports new debug
150 communication interfaces and protocols (like IEEE 1149.7) while maintaining backward compatibility with
151 existing legacy technology. This document also provides recommendations for board level mating
152 connectors that support trace via a high-speed parallel interface. In addition, the trace connectors also
153 support legacy debug via an IEEE 1149.1 interface and the newer IEEE 1149.7 interface. See [IEEE01] and
154 [IEEE02] for more details.

155 This document specifies recommendations for different mating connectors including:

- 156 • Low cost connector configurations that supports basic debug and minimal trace
- 157 • A legacy connector that supports basic debug and a single trace channel
- 158 • A new high performance connector that supports basic debug and up to 4 independent trace
159 channels

160 1.1.1 Document Is

161 This document recommends a physical mating connector used to connect the MIPI Debug Interface on a
162 target system (TS) via a debug and test controller (DTC). It includes pin mappings (based on that
163 connector) that support the following debug configurations:

- 164 • IEEE 1149.7 JTAG in 2-pin mode (Narrow JTAG) debug control
- 165 • IEEE 1149.7 JTAG in 4/5-pin mode or legacy JTAG (IEEE Std 1149.1-2001) (Legacy JTAG)
166 debug control
- 167 • Narrow JTAG debug control with a single 4-data bit PTI
- 168 • Legacy JTAG debug control with a single 4-data bit PTI

169 This document also recommends two physical mating connectors used to connect a target system (TS) to a
170 debug and test controller (DTC) that supports trace capture via a MIPI Parallel Trace Interface (PTI)
171 [MIPI01]. The connector recommendations fall into two classes:

- 172 • A legacy connector (38 signal MICTOR) that provides a migration path from previous trace
173 systems to MIPI. This document recommends pin mappings for the legacy (MICTOR) connector
174 that support the following debug functions:
 - 175 • A maximum of 1 channel of high speed parallel trace
 - 176 • A maximum of 16 PTI TRC_DATA signals
 - 177 • A maximum of 1 PTI TRC_CLK signal
- 178 • Standard debug control
 - 179 • via an IEEE 1149.1 interface (with RTCK) or
 - 180 • via an IEEE 1149.7 interface

- 181 • A new MIPI High Speed Parallel Trace (HSPT) connector (60 signal Samtec QSH/QTH) that
182 provides better signal integrity and more desirable physical performance over the legacy
183 MICTOR. This document recommends pin mappings for the new HSPT connector (QSH/QTH)
184 that support the following debug functions:
- 185 • A maximum of 4 channels of high speed parallel trace
 - 186 • A maximum of 40 PTI TRC_DATA signals
 - 187 • A maximum of 4 PTI TRC_CLK signals
 - 188 • Standard debug control
 - 189 • via an IEEE 1149.1 interface (with RTCK) or
 - 190 • via an IEEE 1149.7 interface

191 **1.1.2 Document Is Not**

192 This document is not the recommended pin mapping for any debug function or interface not enumerated in
193 Section 1.1.1.

194 **1.1.3 Related Specifications**

195 Specifications for the debug functions supported by this recommendation are enumerated in Section 3.

196 **1.2 Purpose**

197 As the connector was not part of the original IEEE 1149.1 JTAG standard, a large number of different
198 JTAG connectors have emerged. The recommendation of standard connectors is an attempt to avoid this for
199 the future. Different applications and use cases have different requirements for the connector. The
200 definition is flexible enough to handle all these requirements. This avoids the need for target specific
201 adapters – with an impact on communication speed and reliability.

202 Many debug tools vendors support target systems with high-speed trace interfaces. These tools utilize a
203 number of different mating connectors. This document recommends two connectors for supporting high
204 speed trace and generic debug. The goal is to have this recommendation define a “de facto” industry
205 standard for the trace connection and thus lessen the burden on target system and tools developers that need
206 to support a large number of different mating connections.

207 The first trace connector is the 38-pin MICTOR connector that has previously been used to support trace
208 connections on many systems. A signal to pin mapping for this connector is provided that supports the run
209 control and trace interfaces specified under MIPI. This recommendation provides a migration path for
210 legacy equipment to support MIPI trace and debug interfaces.

211 The second trace connector is a 60-pin QSH/QTH connector. This connector provides for more and/or
212 wider trace interfaces, has better electrical characteristics and has a wider range of PCB mounting options
213 than the MICTOR and is the recommended connector to new DTCs and target systems.

214 **2 Terminology**

215 **2.1 Definitions**

216 **Narrow JTAG:** IEEE 1149.7 JTAG in 2-pin mode (T4/T5 class TAP.7 of IEEE 1149.7).

217 **Wide JTAG:** IEEE 1149.7 JTAG in 4/5-pin mode (T0-T3 class TAP.7 of IEEE 1149.7) or legacy
218 JTAG (IEEE Std 1149.1-2001).

219 **2.2 Abbreviations**

220 e.g. For example

221 p/n Part Number

222 **2.3 Acronyms**

223 DTC Debug and Trace Controller

224 DTS Debug and Test System

225 HSPT High Speed Parallel Trace

226 ISTO Industry Standards and Technology Organization

227 JTAG Joint Test Access Group

228 MIPI Mobile Industry Processor Interface

229 PCB Printed Circuit Board

230 PTI MIPI Parallel Trace Interface

231 TS Target System

232 T&D Test and Debug

233 **3 References**

- 234 [ARM01] ARM IHI 0014N, *Embedded Trace Macrocell™ ETMv1.0 to ETMv3.4: Architecture*
235 *Specification*, ARM Limited, 8 February 2006.
- 236 [IEEE01] IEEE 1149.1™-2001, *IEEE Standard Test Access Port and Boundary-Scan Architecture*,
237 ISBN 0-7381-2944-5, Institute of Electrical and Electronics Engineers, 14 June 2001.
- 238 [IEEE02] IEEE 1149.7™-2009, *IEEE Standard for Reduced-Pin and Enhanced-Functionality Test*
239 *Access Port and Boundary-Scan Architecture*, Institute of Electrical and Electronics
240 Engineers, 9 December 2009.
- 241 [ISTO01] IEEE-ISTO 5001™-2003, *The Nexus 5001 Forum™ Standard for a Global Embedded*
242 *Processor Debug Interface*, Version 2.0, IEEE-Industry Standards and Technology
243 Organization, 23 December 2003.
- 244 [MIPI01] *MIPI Alliance Standard for Test & Debug – Parallel Trace Interface*, version 1.00, MIPI
245 Alliance, Inc., 19 December 2006.

246 **4 Signal Descriptions**

247 Table 1 contains a summary of all the signal names used to define the pin mappings for all MIPI
248 recommended connectors.

249

Table 1 Signal Descriptions

| Signal(s) | Type and Direction at Board Header | Reference Voltage | Description |
|------------------|------------------------------------|-------------------|--|
| VREF_DEBUG | Analog output | NA | Debug port reference voltage. The pin is used to adjust the DTC input and output buffers to the target voltage. Connected with a resistor to target VCC for I/O buffers driving the debug communications interface and A.C. grounded (Option 1 in Figure 1) with a capacitor or directly connected to target VCC (Option 2 in Figure 1). In the case of Option 1 the resistor shall not have a value greater than 1K Ohms. The capacitor is required for A.C. grounding the cable. |
| VREF_TRACE | Analog output | NA | Trace port reference voltage. Connected with a resistor to target VCC for I/O buffers driving the trace interface and current limited (Option 1 in Figure 2) with a resistor or directly connected to target VCC (Option 2 in Figure 2). In the case of Option 1 the resistor shall not have a value greater than 1K Ohms. |
| TCK | In or Out ² | VREF_DEBUG | IEEE 1149.1 JTAG signals. nTRST is active low signal (sometimes referenced as TRST*). |
| TMS | Input | VREF_DEBUG | |
| TDI ¹ | Input | VREF_DEBUG | |
| TDO ¹ | Output | VREF_DEBUG | |
| nTRST | Input | VREF_DEBUG | |
| RTCK | Output | VREF_DEBUG | Return Test Clock. |
| TMSC | In/Out | VREF_DEBUG | IEEE 1149.7 bi-directional data signal |
| TCKC | In or Out | VREF_DEBUG | IEEE 1149.7 clock signal can be driven from the DTC or the TS |
| TRIGIN | Input | VREF_DEBUG | External debug halt request |
| TRIGOUT | Output | VREF_DEBUG | External debug halt acknowledge |

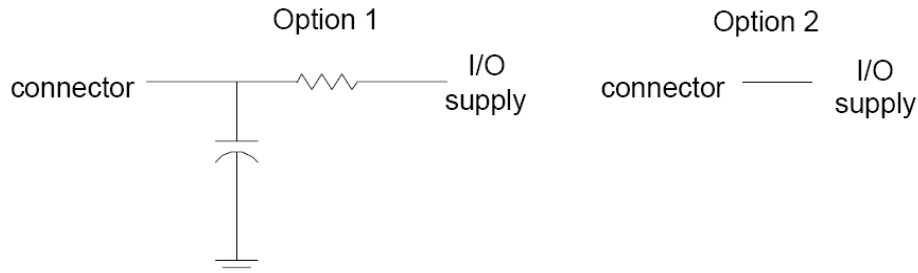
| Signal(s) | Type and Direction at Board Header | Reference Voltage | Description |
|------------------------|------------------------------------|-------------------|--|
| nRESET | Open Drain | VREF_DEBUG | Target reset signal. Open drain active low signal. May be used bi-directional to drive or sense the target reset signal. Usually driven by DTS to reset target system. The TS is responsible for providing a pull up to VREF_DEBUG on this signal to establish a logic one. This pull-up may be outside chips or within chips. The resistor shall not have a value less than 1K Ohms. The capacitor may be present on the TS to provide the power up reset signal. |
| nTRST_PD | Input | VREF_DEBUG | Test Reset Pull-Down. Same function as nTRST, but with pull-down resistor on target. This is an active low signal (sometimes referenced as TRST_PD*). |
| TRC_CLK[N:0] | Output | VREF_TRACE | PTI Trace clock pins. If unused these should be connected to ground or driven to a low logic level. |
| TRC_DATA[N:0] | Output | VREF_TRACE | PTI Trace data pins. Any unused TRC_DATA pin should be tied to ground. |
| EXT | In/Out | VREF_DEBUG | Implementation defined debug application signals that can be used for non-specified functions. |
| TRC_EXT | In/Out | VREF_TRACE | Implementation defined trace sideband signal. |
| Target Presence Detect | Out | VREF_DEBUG | This signal can be used by the debug tools to indicate that an active target system is connected. See Appendix A for details. If this feature is not required this signal should be tied to ground. |

250 **Notes:**

- 251 1. *When implemented in an IEEE 1149.7 environment, the signals TDI, TDO, and RTCK may be multiplexed with a generic debug application (they function*
252 *as an EXT).*
- 253 2. *The IEEE 1149.7 signal TCK may be sourced by the DTC or the Target System.*

254 **4.1 Reference Voltage Pins**

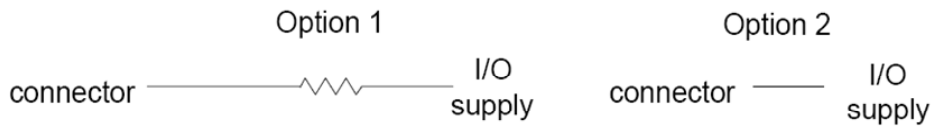
255 Figure 1 and Figure 2 show the different options for configuring the reference voltages for the debug and
 256 trace interfaces on the connector.



257

258

Figure 1 VREF_DEBUG Options



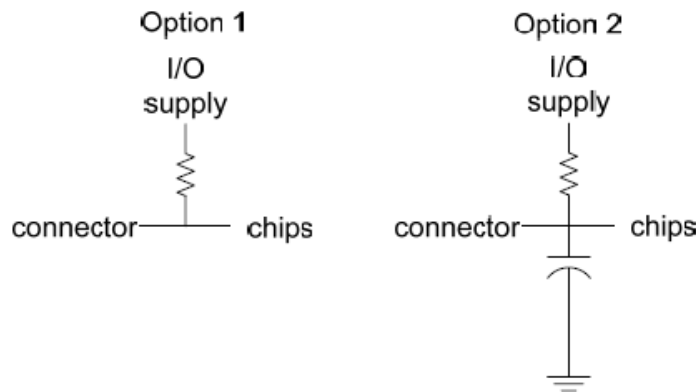
259

260

Figure 2 VREF_TRACE Options

261 **4.2 nRESET**

262 Figure 3 shows how the open drain signal nRESET should be handled on the PCB. Note that when
 263 nRESET is supported on the connector and target system the DTC should not be connected to the TS when
 264 the TS is powered. The “hot connects” may result in unintended resets of the target system.



265

266

Figure 3 nRESET Signal Handling

267 **4.3 nTRST_PD and nTRST**

268 In target systems with multiple discrete devices, it is possible to have a mixture of devices that support only
 269 nTRST_PD or nTRST. The recommendation is to support such systems with a connector configuration and
 270 a DTC that have independent nTRST_PD and nTRST signals. The device level nTRST_PD and nTRST
 271 signals are then routed to the correct pins on the header. There may be scenarios where independent
 272 nTRST_PD and nTRST pins cannot be supported. The following list has some examples:

- 273 • 10-pin header required (only one debug reset signal is available)
- 274 • DTC does not have dual nTRST_PD/nTRST support

275 If required, it is possible to combine nTRST_PD and nTRST and present them as a single pin on the
 276 connector, but system designers should be aware of the functional limitations imposed by this merger. The
 277 IEEE 1149.7 documentation should be consulted, but the following list is a summary of the limitations:

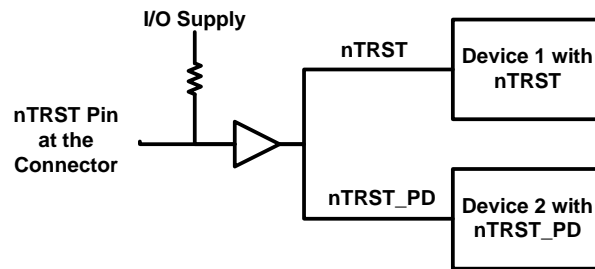
- 278 • Combined connector pin functions as nTRST_PD
 - 279 • Devices with nTRST_PD input
 - 280 • No change in the behavior of the debug and test interface
 - 281 • Devices with nTRST input
 - 282 • Debug and test interface operates in a mode that is not compliant with IEEE 1149.1
 - 283 • The reset is asserted by default.
 - 284 • DTC must be able to drive nTRST_PD pin high to enable the debug interface
- 285 • Combined connector pin functions as nTRST
 - 286 • Devices with nTRST_PD input
 - 287 • Debug and test interface operates in a mode that is not compliant with IEEE 1149.7
 - 288 • The reset is NOT asserted by default
 - 289 • Debug and test logic is not immune to extraneous noise in the system
 - 290 • DTC must be able to pulse nTRST low to reset the interface
 - 291 • Devices with nTRST
 - 292 • No change in the behavior of the debug and test interface

293 Section 4.3.1 provides a recommendation for merging nTRST_PD and nTRST at the board level.

294 **4.3.1 Merging nTRST_PD and nTRST at the Board Level**

295 Since the nTRST signal and nTRST_PD signal have different default (internal pull-up/pull-down) values,
 296 they cannot be tied together. The different logic levels conflict with each other and will drive the resultant
 297 signal to an undefined level. Consequently the TRST* and nTRST_PD signals must be kept separate until
 298 they reach a driver that overdrives the internal pull-up/pull-down values creating the correct logic level.

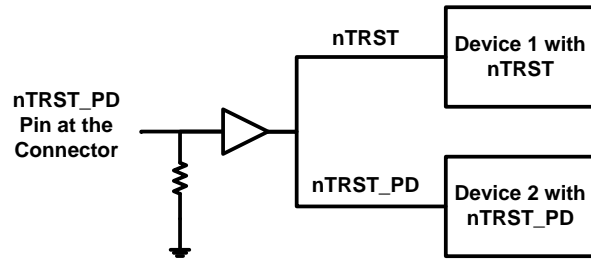
299 Figure 4 and Figure 5 show examples of how board level buffers and pull-ups can be used to merge the
 300 nTRST_PD and nTRST functions to a single pin on the connector.



301

302

Figure 4 nTRST and nTRST_PD Merged as nTRST



303

304

Figure 5 nTRST and nTRST_PD Merged as nTRST_PD

305 **4.4 Exclusive Two-Pin IEEE 1149.7**

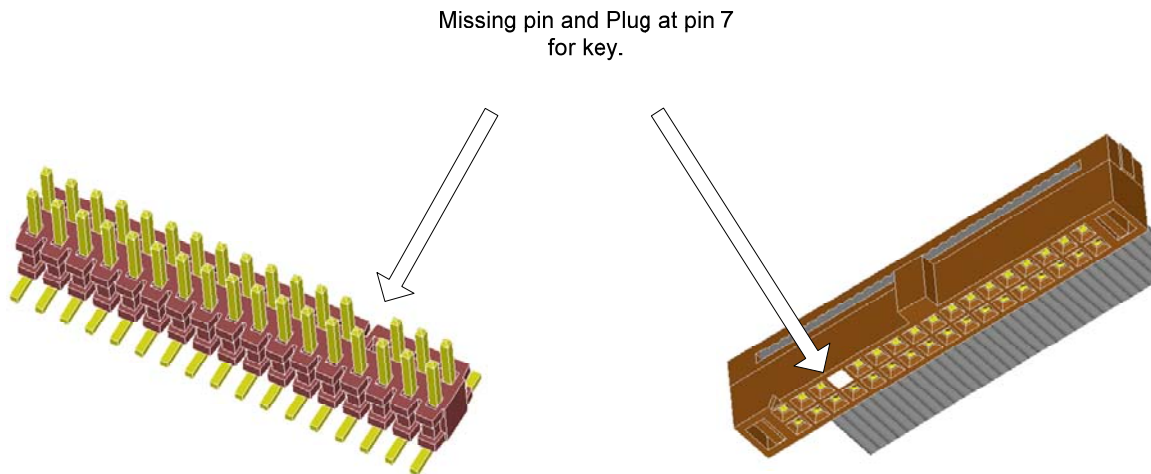
306 It is possible for a MIPI debug connector to be connected to a system that initializes (boots) with a two-pin
 307 IEEE 1149.7 interface. If this type of target system does not provide an nTRST_PD input, then the
 308 nTRST_PD connector pin shall be connected to ground through a resistor.

309 5 Basic Debug Connector

310 A scalable 0.05 inch connector provides an inexpensive, small and robust target connection and is available
 311 in many variants (including lockable ones) from multiple connector vendors. The pin mapping allows
 312 scaling the connection to meet different requirements. This includes very small footprint connections
 313 (down to 10 pins), legacy JTAG support (including vendor specific pins) and system level trace support
 314 (STM). A key pin (pin removed from target connector) enforces polarization. This allows more flexibility
 315 in the connector type and size. It also enables the connection of a larger DTS connector to a smaller TS
 316 connection.

317 5.1 Connector Type

318 The 0.05 inch connector is available from many sources. It is usually offered as standard dual row header
 319 1.27mm x 1.27mm with 0.4mm square pins. Connectors with special locking or polarization may not be
 320 compatible with all debug controllers. Figure 6 contains illustrations of the PCB and cable end connectors.



321
322

323 **Figure 6 Basic Debug Connector (34-pin)**

324 5.1.1 Connector Sources

325 The following Samtec identifiers are examples only. Other vendors provide compatible hardware.

- 326 • Samtec FTSH (SMT Mount)
 - 327 • Horizontal or vertical
 - 328 • Without shroud, with shroud or with ejector shroud
 - 329 • With or without keying
- 330 • Samtec FTSH (Through Hole)
 - 331 • Straight or right Angle
 - 332 • Without shroud, with shroud or with ejector shroud
 - 333 • With or without keying

- 334 • Samtec EHF (Ejector Header)
- 335 • Straight or surface mount or right angle

336 **5.1.1.1 PCB Connector**

337 Table 2 shows the Samtec part number templates for the recommended PCB mounted connectors on the
338 target system. These are templates only and do not address the all of the compatible board connectors
339 available.

340 **Table 2 PCB Mounted Connector Part Number Templates**

| Samtec Part Numbers ¹ | Description |
|--|---|
| FTSH-105-01-<Plating Option>-D<Row Option>-007 | 10-way with pin 7 omitted |
| FTSH-110-01-<Plating Option>-D<Row Option>-007 | 20-way with pin 7 omitted |
| FTSH-117-01-<Plating Option>-D<Row Option>-007 | 34-way with pin 7 omitted |
| FTSH-105-01-<Plating Option>-D<Row Option>-K-007 | 10-way with keyed shroud, pin 7 omitted |
| FTSH-110-01-<Plating Option>-D<Row Option>-K-007 | 20-way with keyed shroud, pin 7 omitted |
| FTSH-117-01-<Plating Option>-D<Row Option>-K-007 | 34-way with keyed shroud, pin 7 omitted |
| EHF-105-01-<Plating Option>-D-<Locking Clip>-007 | 10-way with ejector head, pin 7 omitted |
| EHF-110-01-<Plating Option>-D-<Locking Clip>-007 | 20-way with ejector head, pin 7 omitted |
| EHF-117-01-<Plating Option>-D-<Locking Clip>-007 | 34-way with ejector head, pin 7 omitted |

341 **Notes:**

- 342 1. *These part numbers are generic templates. Specific part numbers are generated by the vendor when*
343 *customers order specific variants of the connector. Contact Samtec for more details.*

344 **5.1.1.2 Cable Connector**

345 Table 3 shows the Samtec part number templates for the recommended cable end/adaptor connectors on the
346 DTC. These are templates only and do not address the all of the compatible connectors available.

347 **Table 3 Cable Connector Part Number Templates**

| Samtec Part Numbers ¹ | Description |
|---|--|
| SFMC-105-<Lead Style Option>-S-D-PK-07-N | 10-way surface mount with pin 7 filled |
| SFMC-110-<Lead Style Option>-S-D-PK-07-N | 20-way surface mount with pin 7 filled |
| SFMC-117-<Lead Style Option>-S-D-PK-07-N | 34-way surface mount with pin 7 filled |
| FFSD-05-<Cable Head Option>-<Length>-01-N-PK-07-N | 10-way cable with key and pin 7 filled |
| FFSD-10-<Cable Head Option>-<Length>-01-N-PK-07-N | 20-way cable with key and pin 7 filled |
| FFSD-17-<Cable Head Option>-<Length>-01-N-PK-07-N | 34-way cable with key and pin 7 filled |

348 **Notes:**

- 349 1. *These part numbers are generic templates. Specific part numbers are generated by the vendor when*
350 *customers order specific variants of the connector. Contact Samtec for more details.*

351 **5.2 Pin Mapping**

352 The pin mapping allows different sizes for extending JTAG functionality or trace features. If legacy JTAG
353 and trace are needed then trace pins are moved from the standard position (pins 12 to 20) to the second
354 variant (pins 22 to 30) with similar pin mapping. This allows minimum size target connectors for all
355 common use cases. Connector sizes of 10, 20 and 34 pins are the recommended connector/cable widths.
356 Unused pins may be used for vendor specific signals.

357 **5.2.1 Rules for Pin Mapping**

358 Designers must review the system requirements in order to determine the connector configuration. The
359 following requirements need to be considered, and then Table 4 should be consulted to determine which
360 header width and pin mapping is appropriate.

- 361 • Narrow or Standard JTAG (or both)
- 362 • Trace Support
- 363 • nTRST_PD, nTRST and nRESET (none, one, two or all three)

364 **5.2.2 Recommended Pin Mappings**

365 Table 4 shows the recommended pin mappings for common use cases.

366

Table 4 MIPI Recommended Pin Mapping for Basic Debug

| All | Pin# | Pin# | 10-pin | 10-pin | 10-pin | 10-pin | 20-pin | 20-pin | 34-pin |
|-------------------------|------|------|---------------|--------------|-----------------|-------------|------------------|---------------------|------------------|
| | | | JTAG + nRESET | JTAG + nTRST | JTAG + nTRST_PD | Narrow JTAG | JTAG | Narrow JTAG + Trace | JTAG + Trace |
| VREF_DEBUG ¹ | 1 | 2 | TMS | TMS | TMS | TMSC | TMS | TMSC | TMS |
| GND | 3 | 4 | TCK | TCK | TCK | TCKC | TCK | TCKC | TCK |
| GND | 5 | 6 | TDO | TDO | TDO | EXT | TDO | EXT | TDO |
| KEY ² | 7 | 8 | TDI | TDI | TDI | nTRST_PD | TDI | nTRST_PD | TDI |
| Target Presence Detect | 9 | 10 | nRESET | nTRST | nTRST_PD | nRESET | nRESET | nRESET | nRESET |
| GND ³ | 11 | 12 | | | | | RTCK | TRC_CLK | RTCK |
| GND ³ | 13 | 14 | | | | | nTRST_PD | TRC_DATA[0] | nTRST_PD |
| GND | 15 | 16 | | | | | nTRST | TRC_DATA[1] | nTRST |
| GND | 17 | 18 | | | | | TRIGIN (DBGRQ) | TRC_DATA[2] | TRIGIN (DBGRQ) |
| GND | 19 | 20 | | | | | TRIGOUT (DBGACK) | TRC_DATA[3] | TRIGOUT (DBGACK) |
| GND | 21 | 22 | | | | | | | TRC_CLK |
| GND | 23 | 24 | | | | | | | TRC_DATA[0] |
| GND | 25 | 26 | | | | | | | TRC_DATA[1] |
| GND | 27 | 28 | | | | | | | TRC_DATA[2] |
| GND | 29 | 30 | | | | | | | TRC_DATA[3] |
| GND | 31 | 32 | | | | | | | TRC_EXT |
| GND | 33 | 34 | | | | | | | VREF_TRACE |

367 **Notes:**

368 1. A.C. grounded with capacitor or direct VCC connection.

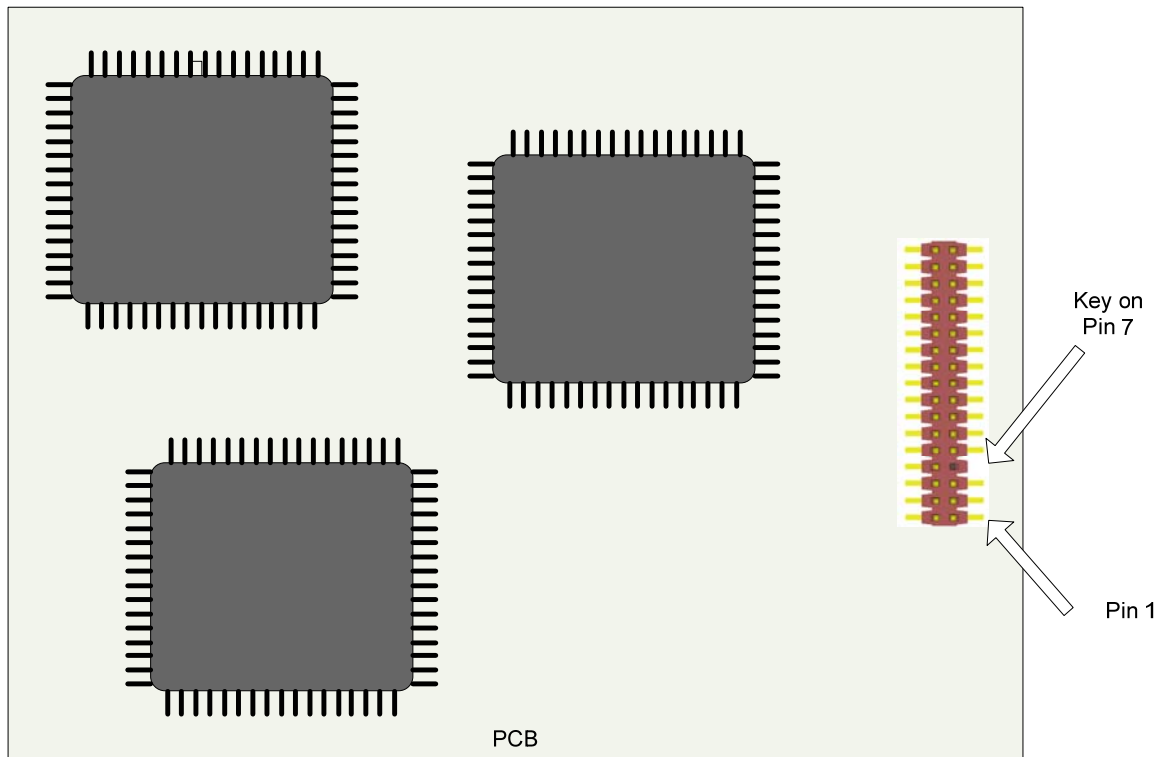
369 2. Pin removed from target connector, grounded in cable.

- 370 3. *ARM Ltd. allows the DTC to supply power to the TS via these pins. This feature is not supported in the MIPI connector.*

371 5.2.3 Physical Orientation of the Connector on the PCB

372 The physical orientation of the connector is important for proper board and DTC design. The following
 373 recommendations define how to place the Basic Debug Connector on the PCB with the target system.

- 374 • Place the even numbered pins of the Basic Debug Connector closest to the Target System(s) that
 375 are supported through the connector. See Figure 7 for an illustration. Note that this orientation is
 376 not the same as the HSPT Connector as described in Section 6.1.7.
- 377 • PCB designers should consult DTC vendor documentation to determine if there are any board
 378 clearance issues related to the DTC cable-end connector



379
 380

381 **Figure 7 Basic Debug Orientation on the PCB (34-pin Example)**

382 5.2.4 Cable-end Design Recommendations

383 DTC vendors may implement cable-end connectors with various physical orientations.

- 384 • Vertical - Cable to the DTC exits the connector housing perpendicular to PCB surface
- 385 • Right-angle – Cable to the DTC exits the connector housing parallel to the PCB surface

386 For right-angle cable-end connectors, the cable interface to the connector should overhang the odd
 387 numbered pins of the connector.

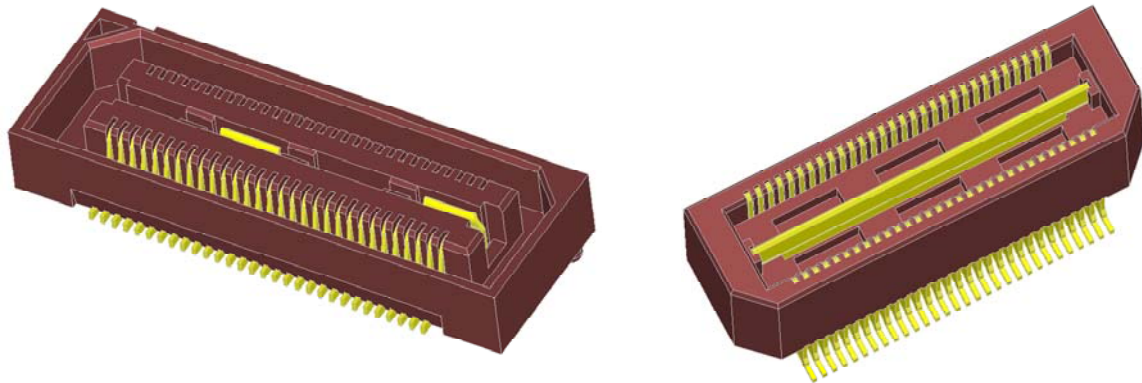
388 6 High Speed Parallel Trace Connectors

389 There are two HSPT connectors discussed in this document. This recommendation promotes a high
 390 performance connector with 60 data signal. This connector allows for a rich pin mapping that can support
 391 the multiple PTI channels that are present in today's complex systems. It also supports a wide variety of
 392 mounting and cable-end options.

393 Many older systems support high speed trace via the 38 pin MICTOR. The PCB mounting limitations
 394 ("through hole") and limited number of data signals make this connector less desirable. While a signal
 395 mapping is provided for the MICTOR, the goal is to have the QSH/QTH become the standard moving
 396 forward.

397 6.1 Recommended HSPT Connector

398 The recommended HSPT connector is the Samtec QSH/QTH family with two rows of 30 pins. All 60 pins
 399 can be dedicated to trace and debug signals. The 01 lead and 5mm stacking height are the recommended
 400 options. Other stacking height options are supported for the PCB and cable-end connections. Figure 8
 401 contains illustrations of the PCB and cable end connectors (QSH and QTH).



402
 403

404 **Figure 8 QSH and QTH Connectors**

405 6.1.1 PCB Connector

406 Table 5 shows the recommended connectors for mounting on the PCB that supports the target system.

407 **Table 5 PCB Mounted Connectors**

| Samtec Part Numbers ¹ | Mount Angle | Mount Type |
|--|-------------|------------|
| QSH-030-01-<Plating Option>-D-<Alignment Pin>-<Other Option> | Vertical | Surface |
| QSH-030-01-<Plating Option>-D-EM<Thickness>-<Other Option> | Edge | Surface |

408 **Notes:**

409 1. Consult Samtec for details on the part numbers.

410 6.1.2 Cable Connector

411 Table 6 shows the recommended connectors for the DTC cable or adaptor boards for DTC connection.

412

Table 6 Cable or DTC Adaptor Connectors

| Samtec Part Numbers ¹ | Mount Angle | Mount Type |
|--|-------------|------------|
| QTH-030-01-<Plating Option>-D-<Alignment Pin>-<Other Option> | Vertical | Surface |
| QTH-030-01-<Plating Option>-D-EM<Thickness>-<Other Option> | Edge | Surface |

413

Notes:

414

1. Consult Samtec for details on the part numbers.

415

6.1.3 Connector Options

416

Table 7 summarizes the other cable options that are supported under this recommendation.

417

Table 7 Connector Options

| Option | Summary |
|----------------|---|
| Plating Option | -L = Gold -F = Gold Flashing |
| Alignment Pin | The catalog connectors come with alignment pins (-A) but these connectors can be special ordered without them or with locking clips |
| Other Option | These specify PCB manufacturing parameters such as Tape & Reel or Pick & Place |

418

6.1.4 Connector Pin Mapping

419

Table 8 shows the generic pin mapping for the QSH/QTH connector. This mapping supports a maximum of four PTI channels. Note, the center ground plane must be connected to ground on the PCB.

420

421

Table 8 QSH/QTH Pin Mapping with a Maximum of 4 PTIs

| Signal ¹ | Pin# | Pin# | Signal ¹ |
|------------------------|------|------|-----------------------------------|
| VREF_DEBUG | 1 | 2 | TMS/TMSC |
| TCK | 3 | 4 | TDO/EXTA |
| TDI/EXTB | 5 | 6 | nRESET |
| RTCK/EXTC | 7 | 8 | nTRST_PD |
| nTRST/EXTD | 9 | 10 | EXTE/TRIGIN |
| EXTF/TRIGOUT | 11 | 12 | VREF_TRACE ² |
| TRC_CLK[0] | 13 | 14 | TRC_CLK[1] |
| Target Presence Detect | 15 | 16 | GND |
| TRC_DATA[0][0] | 17 | 18 | TRC_DATA[1][0] or TRC_DATA[0][20] |
| TRC_DATA[0][1] | 19 | 20 | TRC_DATA[1][1] or TRC_DATA[0][21] |
| TRC_DATA[0][2] | 21 | 22 | TRC_DATA[1][2] or TRC_DATA[0][22] |
| TRC_DATA[0][3] | 23 | 24 | TRC_DATA[1][3] or TRC_DATA[0][23] |
| TRC_DATA[0][4] | 25 | 26 | TRC_DATA[1][4] or TRC_DATA[0][24] |
| TRC_DATA[0][5] | 27 | 28 | TRC_DATA[1][5] or TRC_DATA[0][25] |
| TRC_DATA[0][6] | 29 | 30 | TRC_DATA[1][6] or TRC_DATA[0][26] |
| TRC_DATA[0][7] | 31 | 32 | TRC_DATA[1][7] or TRC_DATA[0][27] |

| Signal ¹ | Pin# | Pin# | Signal ¹ |
|-----------------------------------|------|------|---|
| TRC_DATA[0][8] | 33 | 34 | TRC_DATA[1][8] or TRC_DATA[0][28] |
| TRC_DATA[0][9] ³ | 35 | 36 | TRC_DATA[1][9] ³ or TRC_DATA[0][29] ³ |
| TRC_DATA[3][0] or TRC_DATA[0][10] | 37 | 38 | TRC_DATA[2][0] or TRC_DATA[1][10] or TRC_DATA[0][30] |
| TRC_DATA[3][1] or TRC_DATA[0][11] | 39 | 40 | TRC_DATA[2][1] or TRC_DATA[1][11] or TRC_DATA[0][31] |
| TRC_DATA[3][2] or TRC_DATA[0][12] | 41 | 42 | TRC_DATA[2][2] or TRC_DATA[1][12] or TRC_DATA[0][32] |
| TRC_DATA[3][3] or TRC_DATA[0][13] | 43 | 44 | TRC_DATA[2][3] or TRC_DATA[1][13] or TRC_DATA[0][33] |
| TRC_DATA[3][4] or TRC_DATA[0][14] | 45 | 46 | TRC_DATA[2][4] or TRC_DATA[1][14] or TRC_DATA[0][34] |
| TRC_DATA[3][5] or TRC_DATA[0][15] | 47 | 48 | TRC_DATA[2][5] or TRC_DATA[1][15] or TRC_DATA[0][35] |
| TRC_DATA[3][6] or TRC_DATA[0][16] | 49 | 50 | TRC_DATA[2][6] or TRC_DATA[1][16] or TRC_DATA[0][36] |
| TRC_DATA[3][7] or TRC_DATA[0][17] | 51 | 52 | TRC_DATA[2][7] or TRC_DATA[1][17] or TRC_DATA[0][37] |
| TRC_DATA[3][8] or TRC_DATA[0][18] | 53 | 54 | TRC_DATA[2][8] or TRC_DATA[1][18] or TRC_DATA[0][38] |
| TRC_DATA[3][9] or TRC_DATA[0][19] | 55 | 56 | TRC_DATA[2][9] or TRC_DATA[1][19] or TRC_DATA[0][39] |
| GND | 57 | 58 | GND |
| TRC_CLK[3] | 59 | 60 | TRC_CLK[2] |

422 **Notes:**

- 423 1. All unconnected signals must be tied to ground.
- 424 2. This configuration supports four independently clocked PTIs, but they must have the same
425 reference voltage.
- 426 3. The pin mapping may be configured such that independently clocked channels are present on odd
427 pins 17 to 35 and 37 to 55 or even pins 18 to 36 and 38 to 56. For maximum signal integrity in
428 these scenarios, pins 35 and 36 should not be utilized as trace data signals, but should be
429 connected to ground. This decreases the effective width of one or two of the PTI channels, but it
430 minimizes the risk of cross talk between two adjacent asynchronous signals on the connector or
431 PCB.

432 **6.1.5 Supported Pin Mapping Configurations**

433 In order to minimize the complexity of DTC design, a finite set of supported channel configuration are
434 defined. These configuration classes are defined in Table 9.

435

Table 9 Multiple Channel Configurations

| Configuration Class | Debug Signals | Max Chan 0 ¹ | Max Chan 1 ¹ | Max Chan 2 ¹ | Max Chan 3 ¹ | Comment |
|---------------------|---------------|-------------------------|-------------------------|-------------------------|-------------------------|---|
| Class0 | Yes | - | - | - | - | This class is a debug only DTC with cable support for the trace header. |
| Class1 | Yes | 40 | - | - | - | |
| Class2 | Yes | 40 | 20 | - | - | |
| Class3 | Yes | 40 | 20 | 10 | - | |
| Class4 | Yes | 40 | 20 | 10 | 10 | |

436

Notes:

437

1. The number of signals in a channel may be less than the maximum designated.

438

6.1.6 DTC Support for Multiple PTI Mapping

439

DTCs may support multiple classes of pin configurations. The DTC vendor should provide this information to the customer in a readily understandable format. For example, a vendor may have a DTC that supports two independent PTI channels and 32 data signals. The supported input configurations may be 1X32-bit PTI or 2X16-bit PTIs. The vendor could report that the DTC supports Class1 [32] and Class2 [16/16]. A similar DTC that supports a third PTI could report Class1 [32], Class2 [16/16] and Class3 [16/8/8].

440

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6.1.7 Physical Orientation of the Connector on the PCB

445

The physical orientation of the connector is important for proper board and DTC design. The following recommendations define how to place the QSH connector on the PCB with the target system.

446

447

- Place the odd numbered pins of the QSH (1 to 59) closest to the Target System(s) supported through the connector. Note that this orientation is not the same as the Basic Debug Connector as described in Section 5.2.3.

448

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- As DTC vendors may implement cable-end connectors with a right-angle connection (see Section 6.1.8) or other connector housings that extend past the physical boundaries of the PCB connector, the PCB must be clear of components that might interfere with the cable connection to the DTC. Figure 9 shows an example of a clearance issue introduced by improper board layout.

451

452

453

454

- DTC vendors should attempt to minimize the keep-out or low clearance areas required by their cable-end connections.

455

456

- PCB designers should consult DTC vendor documentation to determine the precise dimensions of the low clearance or keep out areas.

457

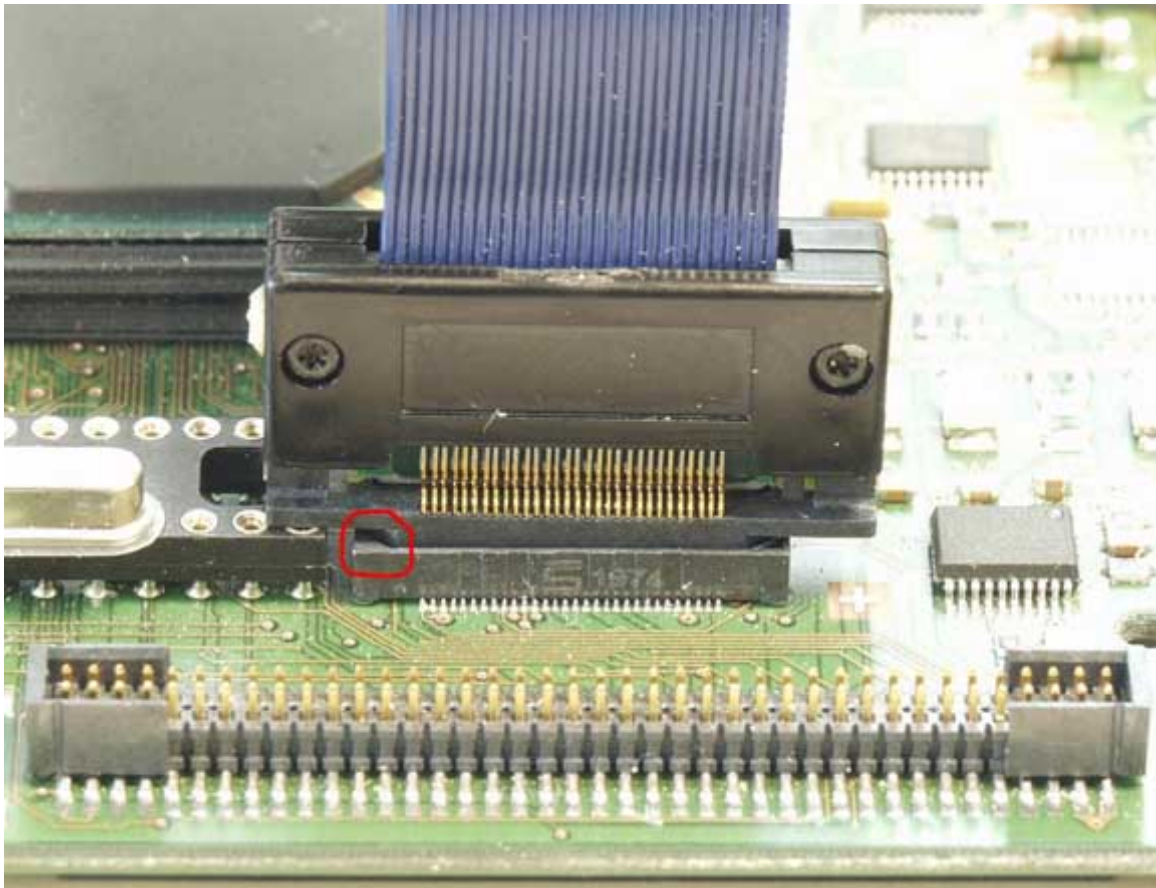
458

- A worst-case keep out area is shown in Figure 10. The dimensions for the keep-out area were derived from the dimensions of the Samtec QCD series cable-end connector with screw down option and the QTH-EM with screw-down option. This is a worst-case description and board designers should always consult DTC vendor documentation.

459

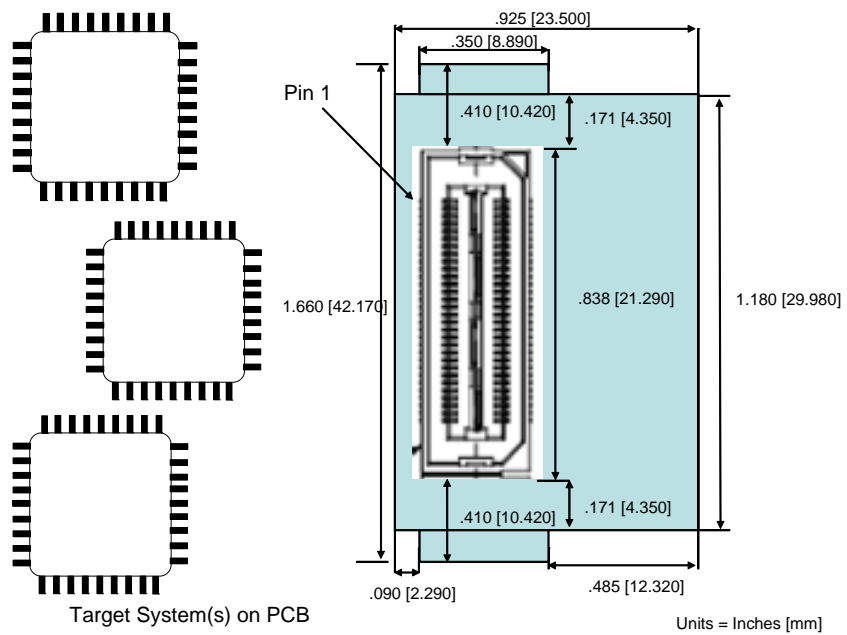
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Figure 9 Cable and Board Clearance Example Showing Improper Board Design Relative to the Clearance Required for Cable-end



465
466

Figure 10 QSH Orientation on the PCB and Low Clearance/Keep-out Area

467 **6.1.8 Cable-end Design Recommendations**

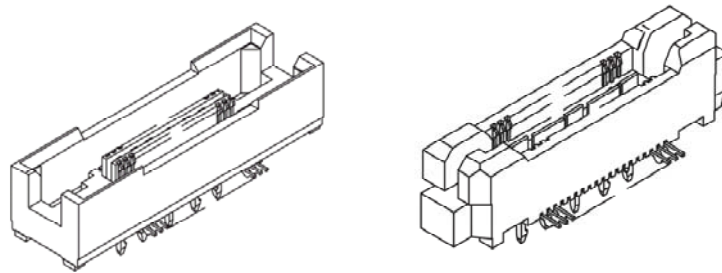
468 As stated in Section 6.1.7, DTC vendors may implement cable-end connectors with various physical
469 orientations.

- 470 • Vertical: Cable to the DTC exits the connector housing perpendicular to PCB surface
- 471 • Right-angle: Cable to the DTC exits the connector housing parallel to the PCB surface

472 For right-angle cable-end connectors, the cable interface to the connector should overhang the even
473 numbered pins (2 to 60) of the connector.

474 **6.2 Legacy Connector**

475 The legacy physical mating connector is the AMP 38 signal Centerline Matched Impedance Connector
476 (MICTOR). Figure 11 contains illustrations of the MICTOR PCB and Cable end connectors.



477
478 **Figure 11 MICTOR PCB (left) and Cable End Connectors**

479 The connectors are listed in Table 10 by AMP (now Tyco Electronics) part number.

480 **Table 10 Legacy (MICTOR) Part Numbers**

| AMP (Tyco) Part Numbers | | Mount Angle | Mount Type | Connector Summary |
|---------------------------|------------|-------------|------------|---|
| RoHS and ELV ¹ | Legacy | | | |
| 2-5767004-2 | 2-767004-2 | Vertical | Surface | Mates with p/n 767006 to create right angle board-to-board configuration. Can also be used as board to cable connector. |
| 5767054-1 | 767054-1 | Vertical | Surface | Board to board or board to cable connection. |
| 5767061-1 | 767061-1 | Vertical | Surface | Board to board or board to cable connection. |
| 5767044-1 | 767044-1 | Surface | Straddle | Board to board or board to cable connection. |

481 **Notes:**

- 482 1. Connectors compliant with Restrictions on Certain Hazardous Substances (RoHS) Directive
483 2002/95/EC and End of Life Vehicles (ELV) Directive 2000/53/EC.

484 6.2.1 Legacy Pin Mapping for Wide JTAG and a Single PTI Channel

485 Table 11 defines the signal to pin mapping for the legacy MICTOR HSPT connector that supports debug
 486 via Wide JTAG and also supports a single PTI with a maximum of 16 TRC_DATA signals. This pin
 487 mapping is fully compatible with legacy debug and trace systems from ARM Ltd. that use the MICTOR
 488 connector. The pin mapping in Table 11 corresponds to the ARM mapping to support Version 3 of the
 489 ETM protocol and provides a way for a PTI interface to share a MICTOR connector with an ETM
 490 interface.

491 **Table 11 Legacy MICTOR with JTAG and a 16 Data Signal PTI**

| Legacy MICTOR with JTAG | | 16 Data Signal PTI | |
|-----------------------------|------|--------------------|---------------------------|
| Signal | Pin# | Pin# | Signal |
| TRC_DATA[0] | 38 | 37 | TRC_DATA[8] ² |
| EXT (TRACECTL) ¹ | 36 | 35 | TRC_DATA[9] ² |
| Logic '1' | 34 | 33 | TRC_DATA[10] ² |
| Logic '0' | 32 | 31 | TRC_DATA[11] ² |
| Logic '0' | 30 | 29 | TRC_DATA[12] ² |
| TRC_DATA[1] ² | 28 | 27 | TRC_DATA[13] ² |
| TRC_DATA[2] ² | 26 | 25 | TRC_DATA[14] ² |
| TRC_DATA[3] ² | 24 | 23 | TRC_DATA[15] ² |
| TRC_DATA[4] ² | 22 | 21 | nTRST |
| TRC_DATA[5] ² | 20 | 19 | TDI |
| TRC_DATA[6] ² | 18 | 17 | TMS |
| TRC_DATA[7] ² | 16 | 15 | TCK |
| EXT (VSupply) ¹ | 14 | 13 | RTCK |
| VREF_TRACE ³ | 12 | 11 | TDO |
| EXT (EXTTRIG) ¹ | 10 | 9 | nRESET |
| TRIGOUT | 8 | 7 | TRIGIN |
| TRC_CLK | 6 | 5 | GND |
| N/C | 4 | 3 | N/C |
| N/C | 2 | 1 | N/C |

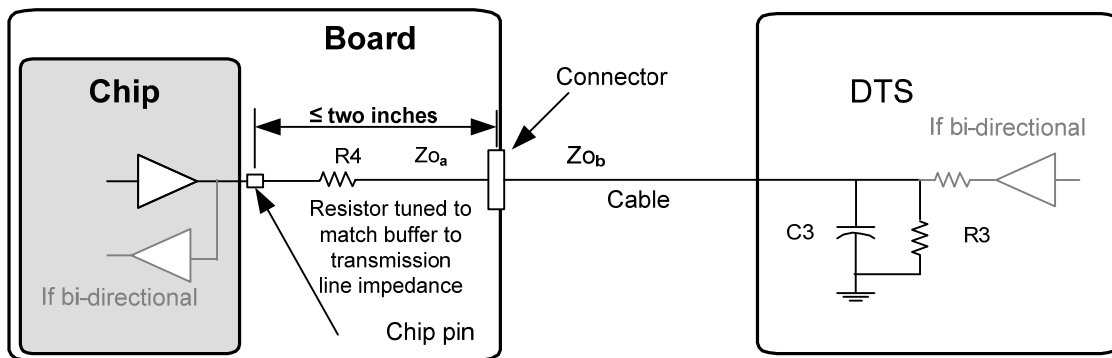
492 **Notes:**

- 493 1. TRACECTL, VSupply and EXTTRIG are signals specified in [ARM01] and are not required to
 494 support a MIPI PTI.
- 495 2. Unused TRC_DATA signals should be tied to ground
- 496 3. VREF_TRACE always provides the reference voltage for the trace interface. If the reference
 497 voltage for the debug interface is not the same, a separate debug only connector must be used.
 498 See Section 7.2 for details.

499 7 Design Considerations

500 7.1 Electrical Recommendations

501 The expectations for high speed signaling (> 25 MHz) is shown in Figure 12.



502

503

Figure 12 Signaling Model for Trace and Other High-speed Pins

504 Component values in Figure 12 are as follows:

- 505 • R3 shall be greater than or equal to 1K Ohms (parasitic load of DTS)
- 506 • C3 shall be smaller than 5pf (parasitic load of DTS)
- 507 • R4 shall be tuned to match the impedance of the buffer to the line impedance Z_{o_a} and Z_{o_b}
- 508 • Z_{o_a} and Z_{o_b} line impedances shall be 50 Ohms \pm 10%

509 7.2 Signal Buffering

510 7.2.1 Buffering Basic Debug Signals

511 On board buffering of basic debug signals is not recommended. This is particularly important since the
 512 newer debug technologies (like IEEE 1149.7) may allow pin functions to change the default direction of the
 513 I/O signals on the debug interface.

514 7.2.2 Buffering Trace (PTI) Signals

515 On board buffering of the trace (PTI) signals is not recommended as it may interfere with the timing
 516 characteristics of the interface and may also cause conflicts with the signal termination implemented by the
 517 DTC.

518 7.3 Debug and Trace Connectors on the Same Target Board

519 It is possible for board designers to provide multiple debug connectors on the same target board. In general,
 520 this would be a standard debug connector for use with run control debug and an HSPT connector for trace.
 521 Several design considerations should be noted when supporting multiple debug connectors.

522 **7.3.1 Debug Signals to Two Connectors**

523 If the DTS and DTC systems to be used for a target system support independent trace and debug
524 connections, it is recommended that the debug signals be routed to the debug connector only, and not to the
525 trace connector. This configuration will eliminate any performance issues with the IEEE 1149.1 or 1149.7
526 interfaces that would be introduced by having PCB traces to both connectors.

527 **7.3.2 Legacy Trace Connector and Multiple Reference Voltages**

528 There is only one reference voltage on the HSPT connector pin mapping that is compatible with ARM
529 ETM (Section 6.2.1). In this scenario, only one reference voltage is available on the connector. If the debug
530 interface and the trace interface of your target system have different reference voltages, a separate debug
531 only connector must be placed on the PCB to allow the DTS and DTC to differentiate the interface reference
532 voltages.

533 **7.4 TRC_DATA Signal Routing on PCB**

534 Great care must be taken when routing high speed trace signals on the PCB. When using the Samtec
535 QSH/QTH connector, PCB designer should consult the Samtec web site for Final Inch® data regarding
536 board layout and routing.

537 **7.5 Overlaying Multiple PTIs on an ASIC Boundary**

538 Many ASICs designs will have multiple modules that must share the pins of a chip level debug port (see the
539 highlighted portion of Figure 13). These modules implement interfaces that have the characteristics of a
540 PTI, but are not true PTI since they are not directly driving pins on the device boundary. The pin
541 constraints for these devices generally prevent all of the modules from having dedicated PTIs. Physical
542 design constraints (e.g. multiple on-chip die) or protocol constraints prevent the merging of trace sources
543 into a single stream that uses a single PTI. These types of systems generally manage the shared PTI using
544 some relatively simple pin multiplexing logic.

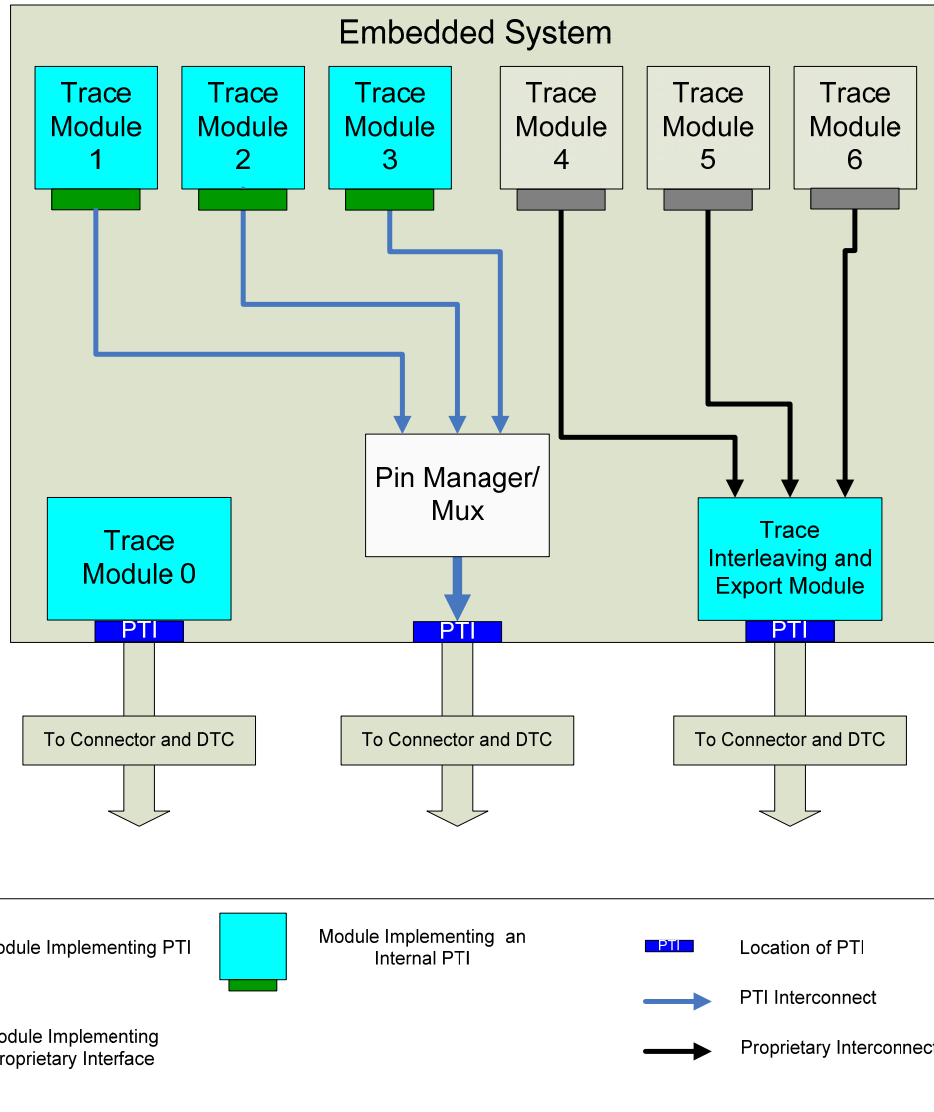


Figure 13 Multiplexed PTIs at the ASIC Level

7.5.1 Simple Shared Interfaces

In general, the simplest approach is to just overlay the PTI interfaces within the SOC with all the clocks sharing the same pin and the corresponding data signals all multiplexed with the same indexes sharing a pin. Table 12 shows a simple overlay of a 10 data single PTI and a 4 data signal PTI that share chip-level debug interface that is 11 pins wide.

Table 12 Simple Multiplexed Pin Mapping

| Pin Number | Mapping for Mode A | Mapping for Mode B |
|------------|--------------------|--------------------|
| 0 | PTI_A(TRC_CLK) | PTI_B(TRC_CLK) |
| 1 | PTI_A(TRC_DATA[0]) | PTI_B(TRC_DATA[0]) |
| 2 | PTI_A(TRC_DATA[1]) | PTI_B(TRC_DATA[1]) |
| 3 | PTI_A(TRC_DATA[2]) | PTI_B(TRC_DATA[2]) |

| Pin Number | Mapping for Mode A | Mapping for Mode B |
|------------|--------------------|--------------------|
| 4 | PTI_A(TRC_DATA[3]) | PTI_B(TRC_DATA[3]) |
| 5 | PTI_A(TRC_DATA[4]) | Not Connected |
| 6 | PTI_A(TRC_DATA[5]) | Not Connected |
| 7 | PTI_A(TRC_DATA[6]) | Not Connected |
| 8 | PTI_A(TRC_DATA[7]) | Not Connected |
| 9 | PTI_A(TRC_DATA[8]) | Not Connected |
| 10 | PTI_A(TRC_DATA[9]) | Not Connected |

553 The simple example poses no issues for the connector because only one trace channel can be active at any
554 given time.

555 7.5.2 Complex Shared Interfaces

556 The complexity increases when simultaneously sharing the port. If PTI_A from the previous example had a
557 configurable export interface width, then it would be possible to have both a narrow PTIA_A and a PTI_B
558 active on the chip interface simultaneously.

- 559 • $PTI_A = TRC_CLK[A] + TRC_DATA[A][3:0]$
- 560 • $PTI_B = TRC_CLK[B] + TRC_DATA[A][4:0]$

561 The device is then capable of supporting several PTI modes:

- 562 • All debug pins dedicated to PTI_A
- 563 • All debug pins dedicated to PTI_B (some are not operational)
- 564 • Debug pins allocated to both PTI_A and PTI_B

565 This flexible debug interface may be very useful for developers, but it poses problems for the signal
566 mapping to the connector. **It should be avoided if at all possible.**

567 The major issue is that all of the ASIC level debug pins are not assigned a monolithic function. At least one
568 of the pins is a TRC_DATA signal in the exclusive modes and a TRC_CLK signal in the simultaneous
569 modes. Since the connector pins (and possible the DTC input interface) are fixed functions (either clock or
570 data, but not both), it is difficult to define a pin mapping for the ASIC signals that can be supported.

571 7.5.3 ASIC Pin Mapping for Simultaneous Shared Interfaces

572 If the ASIC pin mapping is done correctly, it is possible to support the simultaneous trace modes with the
573 MIPI connectors, but under a very severe set of constraints:

- 574 • The chip level debug interface can only support a maximum of two simultaneously active PTIs
575 (PTI_A and PTI_B)
- 576 • At least one of the PTI modules must have configurable export width
- 577 • The DTC must be able to associate TRC_DATA input signals with more than one TRC_CLK
578 input
- 579 • The DTC must be able to accept data that does not follow the signal ordering indexes defined in
580 the connector mapping
- 581 • The DTC must support the support the connector signal TRC_CLK[1]

- 582 • Board designers must take great care to minimize the impact of multiple route for one of the
583 signals
- 584 • The only way to utilize the entire width of the interface is to use a DTC that allows data capture
585 over a signal connected to a clock input on the connector. If this is not possible, the width of the
586 widest PTI will be decreased by one TRC_DATA signal.

587 The generic proposal is to have the ASIC provide a mapping mode where the PTIs share the interface by
588 placing the TRC_CLK signals at opposite ends of the trace interface. The data signals for the first PTI are
589 mapped to the low order pins on the interface with the data indexes incremented. The signals for the second
590 PTI are mapped to the high order bits of the interface with the data indexes decrementing. This provides the
591 greatest flexibility to the system since the widths of the two PTIs can be tuned to provide the desired
592 bandwidth allocation.

593 The proposal requires a simple set of definitions:

- 594 • The pins allocated to for all trace sources are called the Trace Port
- 595 • The Trace Port width is defined as W_t and has pin P[0] to P[$W_t - 1$]
- 596 • PTI_A has the widest data export width w_a
- 597 • PTI_B has the same or narrower data export width w_b

598 Using the previous definitions, the general rules for ASIC level PTI mapping are defined as follows:

- 599 • PTI_A:TRC_CLK is mapped to P[0]
- 600 • PTI_A:TRC_DATA[0] is mapped to P[1]
- 601 • PTI_A:TRC_DATA[w_a] is mapped to P[$w_a + 1$]
- 602 • PTI_B:TRC_CLK is mapped to P[$W_t - 1$]
- 603 • PTI_B:TRC_DATA[0] is mapped to P[$W_t - 2$]
- 604 • PTI_B:TRC_DATA[$w_b - 1$] is mapped to P[$W_t - w_b$]

605 Table 13 expands the example from Table 12 to include a simultaneous shared mode (A+B). Note that the
606 exclusive modes still overlay the TRC_CLK for PTI_A and PTI_B on the same pin. This simple mapping
607 is maintained so that PTI_B can still be received by a DTC that is not capable of supporting a the
608 simultaneous shared export.

609

Table 13 Simultaneous Export Pin Mapping

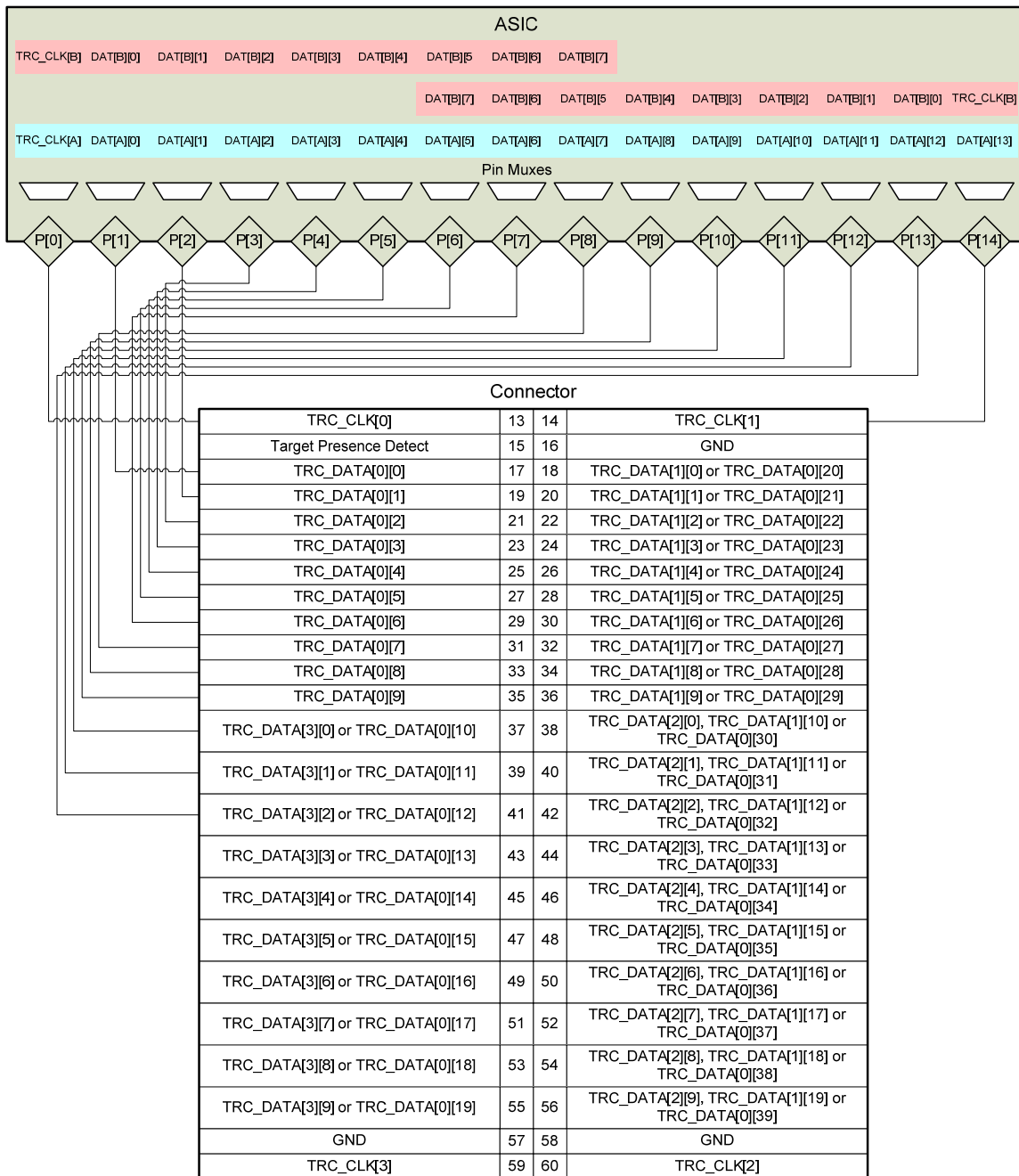
| Pin Number | Mapping for Mode A | Mapping for Mode B | Mapping for Mode A+B |
|------------|--------------------|--------------------|----------------------|
| 0 | PTI_A(TRC_CLK) | PTI_B(TRC_CLK) | PTI_A(TRC_CLK) |
| 1 | PTI_A(TRC_DATA[0]) | PTI_B(TRC_DATA[0]) | PTI_A(TRC_DATA[0]) |
| 2 | PTI_A(TRC_DATA[1]) | PTI_B(TRC_DATA[1]) | PTI_A(TRC_DATA[1]) |
| 3 | PTI_A(TRC_DATA[2]) | PTI_B(TRC_DATA[2]) | PTI_A(TRC_DATA[2]) |
| 4 | PTI_A(TRC_DATA[3]) | PTI_B(TRC_DATA[3]) | PTI_A(TRC_DATA[3]) |
| 5 | PTI_A(TRC_DATA[4]) | Not Connected | PTI_A(TRC_DATA[4]) |
| 6 | PTI_A(TRC_DATA[5]) | Not Connected | PTI_B(TRC_DATA[3]) |
| 7 | PTI_A(TRC_DATA[6]) | Not Connected | PTI_B(TRC_DATA[2]) |
| 8 | PTI_A(TRC_DATA[7]) | Not Connected | PTI_B(TRC_DATA[1]) |
| 9 | PTI_A(TRC_DATA[8]) | Not Connected | PTI_B(TRC_DATA[0]) |
| 10 | PTI_A(TRC_DATA[9]) | Not Connected | PTI_B(TRC_CLK) |

610 **7.5.4 Connector Mapping for Simultaneous Shared Interfaces**

611 The rules for mapping the ASIC pins to the connector are outlined as follows:

- 612 • P[0] is connected to connector pin TRC_CLK[0]
- 613 • P[1] is connected to connector pin TRC_DATA[0][0]
- 614 • P[$W_t - 2$] is connected to connector pin TRC_DATA[0][$W_t - 2$]
- 615 • P[$W_t - 1$] is connected to connector pin TRC_CLK[1]

616 Figure 14 shows a more generic example of the connector signal mapping for a 14 data signal PTI and an 8
 617 data signal PTI. The example uses a 15 signal debug port to show how the signals span two 10 signal
 618 segments on the connector.



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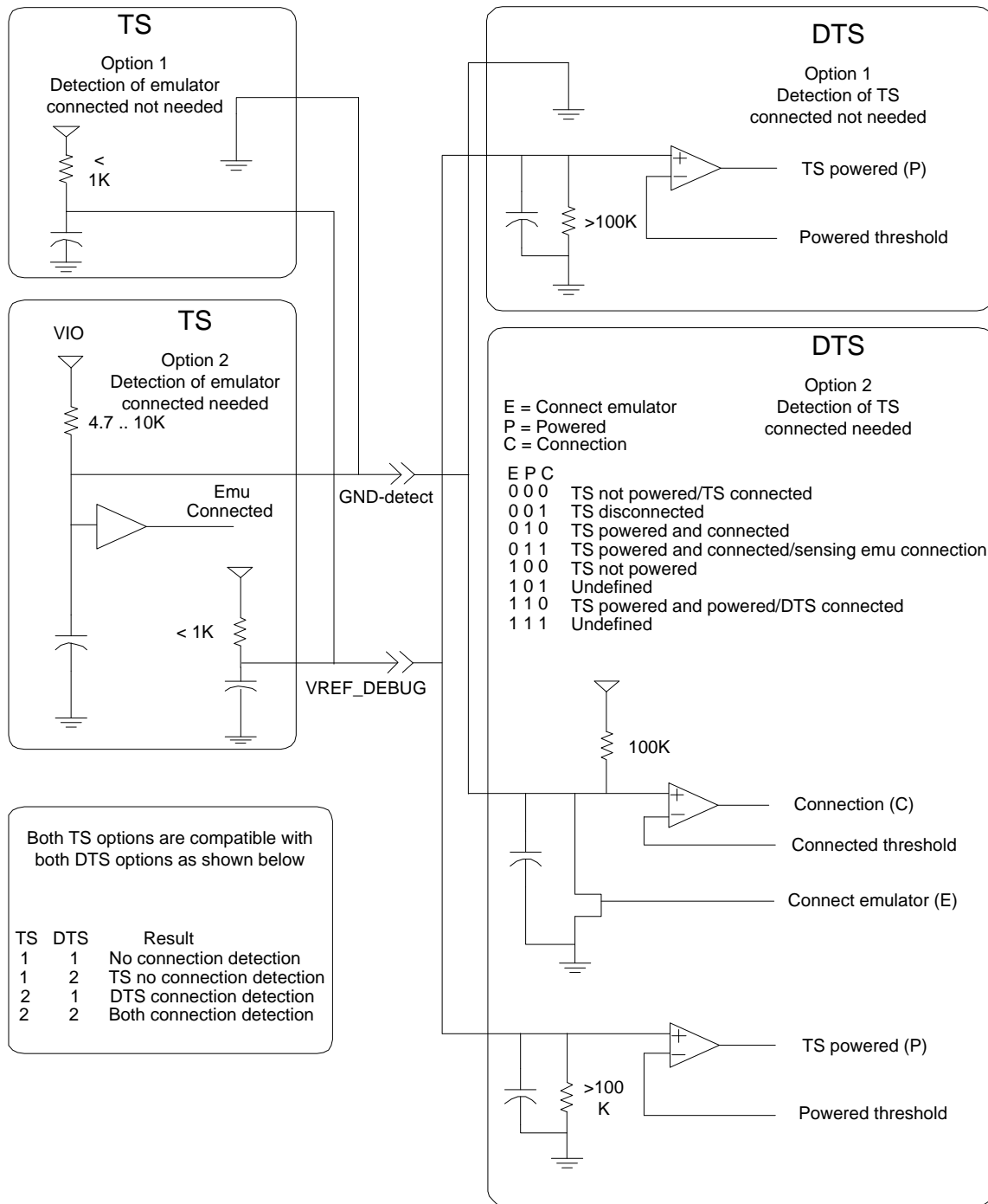
Figure 14 Example of PTI Signal Overlays at the ASIC Boundary

622 **Annex A Debugger and Target Presence Detection**

623 The marked GND-detect pin may be used to detect the presence of the DTS (debug controller) by the TS
624 (target) or the presence of the TS by the DTS. The pin is directly connected to GND if any side does not
625 require detection. The following example circuit allows the detection in both directions with one GND pin.

626 This circuit uses the following premises:

- 627 • If target power is detected, the target is both powered and connected
- 628 • If target power is not detected then the DTS does not drive the connected signal to ground
- 629 • If target power is not detected and the DTS is not driving the connected signal the DTS determines
630 if the DTS is connected by detecting a voltage below the threshold on this signal
- 631 • Once target power is detected the DTS may drive the connected signal to a zero
- 632 • When target power is off, the connected path to the TS power supply appears as a near ground
633 potential



634

635

636

Figure 15 Bi-directional Presence Detect

637 **Annex B ARM ETM Pin Mapping**

638 The ARM ETM is a very popular on-chip debug component. It is anticipated that many systems may
 639 require mapping a MIPI PTI and an ARM ETM interface on the same connector (and device pins). This
 640 appendix to the connector recommendation defines the mapping the ETM output to one or more PTI
 641 channels on the new MIPI HSPT connector. The Table 14 through Table 20 shows the mappings for
 642 ETMv1, ETMv2 and ETMv3 signal protocols.

643 **B.1 Standard ETM Pin Mapping**644 **Table 14 ETMv1/2 to PTI Mapping**

| PTI Signal ($C^1 = 0-3$) | ETMv1 ($W^2 = 4, 8, 16$) | ETMv2 ($W^2 = 4, 8, 16$) |
|----------------------------|----------------------------|----------------------------|
| TRC_CLK[C] | TRACE_CLK | TRACE_CLK |
| TRC_DATA[C][0] | PIPESTAT[0] | PIPESTAT[0] |
| TRC_DATA[C][1] | PIPESTAT[1] | PIPESTAT[1] |
| TRC_DATA[C][2] | PIPESTAT[2] | PIPESTAT[2] |
| TRC_DATA[C][3] | TRACESYNC | PIPESTAT[3] |
| TRC_DATA[C][W+3:4] | TRACEDATA[W-1:0] | TRACEDATA[W-1:0] |

645 **Notes:**

- 646 1. C = PTI Channel Index on the connector
 647 2. W = ETM Port Width

648 The ETMv3 signal protocol has an optional TRACECTL signal. The use of this signal is being deprecated,
 649 but some legacy tools still require it for proper trace capture. When the tools requirements for a system are
 650 known, one of the two pin mappings in Table 15 should be used.

651 **Table 15 ETMv3 to PTI Mapping**

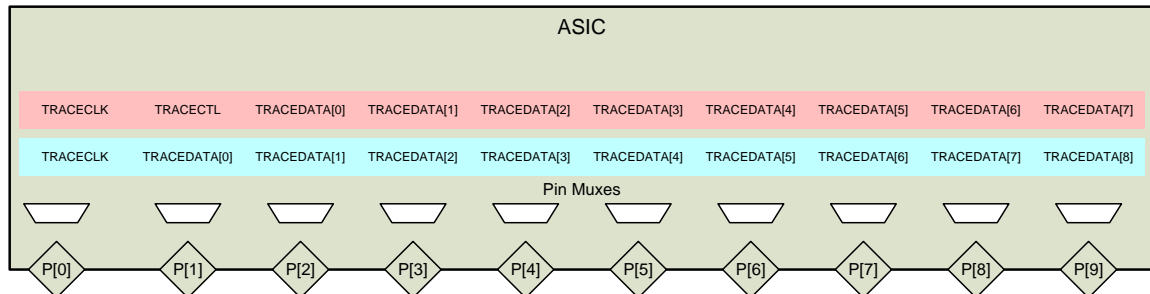
| PTI Signal ($C^1 = 0-3$) | ETMv3 ($W^2 = 1-32$) | ETMv3 ($W^2 = 1-32$) |
|----------------------------|------------------------|------------------------|
| | Recommended | Legacy Only |
| TRC_CLK[C] | TRACE_CLK | TRACE_CLK |
| TRC_DATA[[C][0] | GND | TRACECTL |
| TRC_DATA[[C][1] | TRACEDATA[0] | TRACEDATA[0] |
| | . | |
| | . | |
| | . | |
| TRC_DATA[C][W-2] | TRACEDATA[W-2] | TRACEDATA[W-2] |
| TRC_DATA[C][W-1] | TRACEDATA[W-1] | TRACEDATA[W-1] |

652 **Notes:**

- 653 1. C = PTI Channel Index on the connector
 654 2. W = ETM Port Width

655 There may be scenarios where ASICs and PCBs are required to support both ETMv3 signal formats. Since
 656 ASIC pins are a finite resource, care must be taken at the ASIC level to insure that the overlay of both
 657 signal formats maximizes the utility of the pins assigned to the interface. This can be achieved by assigning

658 the TRACECTL signal to the lowest order data pin when it is required. The trace data signals are then
 659 mapped to the remaining signals on the interface. When TRACECTL is not required, the trace data signals
 660 are mapped beginning at the lowest order data signal on the interface. Figure 16 illustrates this overlay for a
 661 ASIC level trace interface with 10 signals.



662
663

664

Figure 16 ASIC Level Multiplexing with, and without, TRACECTL

665 The overlay method previously described results in the connector signal mappings shown in Table 16. This
 666 type of pin mapping may not be supported natively by many debug tools because the data signal overlay is
 667 not a one-to-one mapping. Adapters may be required to get the proper signal alignment for the tool.

668

Table 16 ETMv3 to PTI Mapping for Overlay Scenario

| PTI Signal ($C^1 = 0-3$) | ASIC Pin Index | ETMv3 ($W^2 = 1-32$) | ETMv3 ($W2 = 1-32$) |
|----------------------------|----------------|------------------------------|-----------------------|
| | | Legacy Mode | No TRACECTL Mode |
| TRC_CLK[C] | 0 | TRACE_CLK | TRACE_CLK |
| TRC_DATA[[C][0] | 1 | TRACECTL | TRACEDATA[0] |
| TRC_DATA[[C][1] | 2 | TRACEDATA[0] | TRACEDATA[1] |
| | | . | |
| | | . | |
| | | . | |
| TRC_DATA[C][W-2] | W-1 | TRACEDATA[W ³ -2] | TRACEDATA[W-2] |
| TRC_DATA[C][W-1] | W | TRACEDATA[W ³ -1] | TRACEDATA[W-1] |

669

Notes:

670

1. C = PTI Channel Index on the connector

671

2. W = ETM Port Width

672

3. For a given number of pins used for the PTI, the Legacy Mode ETM Port Width W has one less data signal than the No TRACECTL Mode.

673

674

B.2 Demultiplexed ETM Pin Mapping

675

The demultiplexed pin mapping requires two (2) PTI channels with a common clock.

676

Table 17 Demultiplexed ETMv1 to PTI Mapping

| PTI Signal ($Ca^1 = 0/2$) | ETMv1 ($W^2 = 4, 8, 16$) | PTI Signal ($Cb1 = 1/3$) | ETMv1 ($W^2 = 4, 8, 16$) |
|-----------------------------|----------------------------|----------------------------|----------------------------|
| TRC_CLK[Ca] | TRACE_CLK | TRC_CLK[Cb] | TRACE_CLK |

| PTI Signal ($Ca^1 = 0/2$) | ETMv1 ($W^2 = 4, 8, 16$) | PTI Signal ($Cb^1 = 1/3$) | ETMv1 ($W^2 = 4, 8, 16$) |
|-----------------------------|----------------------------|-----------------------------|----------------------------|
| TRC_DATA[Ca][0] | PIPESTAT_A[0] | TRC_DATA[Cb][0] | PIPESTAT_B[0] |
| TRC_DATA[Ca][1] | PIPESTAT_A[1] | TRC_DATA[Cb][1] | PIPESTAT_B[1] |
| TRC_DATA[Ca][2] | PIPESTAT_A[2] | TRC_DATA[Cb][2] | PIPESTAT_B[2] |
| TRC_DATA[Ca][3] | TRACESYNC_A | TRC_DATA[Cb][3] | TRACESYNC_B |
| TRC_DATA[Ca][W+3:4] | TRACEDATA_A[W-1:0] | TRC_DATA[Cb][W+3:4] | TRACEDATA_B[W-1:0] |

677

Notes:

678

1. Ca and Cb = PTI Channel Index on the connector. The demultiplexed mapping is supported using symmetric channels on the connector ($a/b = 0/1$ or $2/3$).

679

680

2. W = ETM Port Width.

681

Table 18 Demultiplexed ETMv2 to PTI Mapping

| PTI Signal ($Ca^1 = 0/2$) | ETMv1 ($W^2 = 4, 8, 16$) | PTI Signal ($Cb^1 = 1/3$) | ETMv1 ($W^2 = 4, 8, 16$) |
|-----------------------------|----------------------------|-----------------------------|----------------------------|
| TRC_CLK[Ca] | TRACE_CLK | TRC_CLK[Cb] | TRACE_CLK |
| TRC_DATA[Ca][0] | PIPESTAT_A[0] | TRC_DATA[Cb][0] | PIPESTAT_B[0] |
| TRC_DATA[Ca][1] | PIPESTAT_A[1] | TRC_DATA[Cb][1] | PIPESTAT_B[1] |
| TRC_DATA[Ca][2] | PIPESTAT_A[2] | TRC_DATA[Cb][2] | PIPESTAT_B[2] |
| TRC_DATA[Ca][3] | PIPESTAT_A[3] | TRC_DATA[Cb][3] | PIPESTAT_B[3] |
| TRC_DATA[Ca][W+3:4] | TRACEDATA_A[W-1:0] | TRC_DATA[Cb][W+3:4] | TRACEDATA_B[W-1:0] |

682

Notes:

683

1. Ca and Cb = PTI Channel Index on the connector. The demultiplexed mapping is supported using symmetric channels on the connector ($Ca/Cb = 0/1$ or $2/3$).

684

685

2. W = ETM Port Width.

686

B.3 Multiplexed ETM Pin Mapping

687

With the multiplexed pin mapping, each device pin is multiplexed between two ETM output signals. These are sampled on opposite edges of the trace clock.

688

689

Table 19 Multiplexed ETMv1 to PTI Mapping

| PTI Signal ($C^1 = 0-3$) | ETMv1 ($W^2 = 4, 8, 16$) |
|----------------------------|----------------------------|
| TRC_CLK[C] | TRACE_CLK |
| TRC_DATA[C][0] | PIPESTAT[0] + TRACESYNC |
| TRC_DATA[C][1] | PIPESTAT[1] + TRACEDATA[1] |
| TRC_DATA[C][2] | PIPESTAT[2] + TRACEDATA[2] |
| TRC_DATA[C][3] | TRACEDATA[0,3] |
| TRC_DATA[C][4] | TRACEDATA[4,5] |
| TRC_DATA[C][5] | TRACEDATA[6,7] |
| TRC_DATA[C][6] | TRACEDATA[8,9] |
| TRC_DATA[C][7] | TRACEDATA[10,11] |

| PTI Signal ($C^1 = 0-3$) | ETMv1 ($W^2 = 4, 8, 16$) |
|----------------------------|----------------------------|
| TRC_DATA[C][8] | TRACEDATA[12,13] |
| TRC_DATA[C][9] | TRACEDATA[14,15] |

690 **Notes:**

691 1. C = PTI Channel Index on the connector.

692 2. W = ETM Port Width.

693

Table 20 Multiplexed ETMv2 to PTI Mapping

| PTI Signal ($C^1 = 0-3$) | ETMv2 ($W^2 = 4, 8, 16$) |
|----------------------------|----------------------------|
| TRC_CLK[C] | TRACE_CLK |
| TRC_DATA[C][0] | PIPESTAT[0] + PIPESTAT[3] |
| TRC_DATA[C][1] | PIPESTAT[1] + TRACEDATA[1] |
| TRC_DATA[C][2] | PIPESTAT[2] + TRACEDATA[2] |
| TRC_DATA[C][3] | TRACEDATA[0,3] |
| TRC_DATA[C][4] | TRACEDATA[4,5] |
| TRC_DATA[C][5] | TRACEDATA[6,7] |
| TRC_DATA[C][6] | TRACEDATA[8,9] |
| TRC_DATA[C][7] | TRACEDATA[10,11] |
| TRC_DATA[C][8] | TRACEDATA[12,13] |
| TRC_DATA[C][9] | TRACEDATA[14,15] |

694 **Notes:**

695 1. C = PTI Channel Index on the connector.

696 2. W = ETM Port Width.

697 **Annex C Nexus Pin Mapping**

698 The Nexus 5001 Forum™ has defined a standard for a debug interface that is very popular in the embedded
 699 automotive sector. It is anticipated that many systems may require mapping a MIPI PTI and a Nexus
 700 interface on the same connector (and device pins). This annex to the connector recommendation defines the
 701 mapping the Nexus output interface to one or more PTI channels on the new MIPI HSPT connector. Table
 702 21 and Table 22 show the pin mappings.

703 **Table 21 Nexus Message Interface to PTI Mapping**

| PTI Signal ($C^1 = 0-3$) | Nexus Aux Output ($W^2 = 1-32$) |
|----------------------------|-----------------------------------|
| TRC_CLK[C] | MCKO |
| TRC_DATA[C][0] | MSEO[0] |
| TRC_DATA[C][1] | MSEO[1] |
| TRC_DATA[C][W+1:2] | MDO[W-1:0] |

704 **Notes:**

- 705 1. C = PTI Channel Index on the connector.
 706 2. W = Nexus Port Width.

707 The Nexus standard also defines extended signals used for basic debug functions. These signals can be
 708 mapped to the MIPI connectors using Table 22. The overlay scheme applies to any connector that supports
 709 the designated MIPI signal.

710 **Table 22 Nexus Extended Pin Mapping**

| MIPI Signal Name | Nexus Signal |
|------------------|--------------|
| TRIGIN | EVTI |
| TRIGOUT | EVTO |
| nTRST_PD | RSTI |
| RTCK | RDY |

711